International Journal of Research Studies in Science, Engineering and Technology
Volume 6, Issue 2, 2019, PP 40-47
ISSN 2349-476X
DOI: https://doi.org/10.22259/2349-476X.0602006

Capable Design of a Reversible Categorization Circuit

Balasani Naga Nandini [1], Ganimisetty Uma Sravanthi [1], Linga Sravani[1], Konda Sirisha[1], Sanjay Kumar Suman[2]

[1]IV B.Tech, ECE Dept., Malineni Lakshmaiah Women's Engineering College, Guntur, A.P
[2]Assistant Professor, Malineni Lakshmaiah Women's Engineering College, Guntur, A.P

ABSTRACT

In recent research domains, reversible logic has become an important exposure for low-power consumption and speedier processing. The goal of creating a reversible sorting circuit is to reduce power consumption while maintaining communication reliability. This study presents two efficient sorting circuits that can sort binary values in descending order. The suggested circuits have three or four inputs, each of which has three bits. The comparator was built using Fredkin and Toffoli gates. The suggested switch, which creates a result bit based on the comparator's input, also uses a Fredkin gate. For sorting three inputs, the suggested circuit requires 102 principal reversible gates, 170 gates for sorting four inputs, 195 garbage outputs for three inputs, and 325 garbage outputs for four inputs. 510 quantum cost for 3 inputs and 850 quantum cost for 4 inputs, with hardware complexity of (150 + 246 + 96) for 3 inputs and (250 + 410 + 160) for 4 inputs.

Sorting is employed in various domains in the present period, including pulse generating, counting, and searching procedures. Many studies have been conducted on reversible sequential and combinational circuits, but reversible sorting circuits have yet to be investigated, therefore this could be one of the first in this field.

INTRODUCTION

In VLSI technology, power dissipation is a very important issue. Reversible logic gates are based on reversible operation to reduce the power dissipation of logic circuits based on Landauer's concept where it is proved that for each bit of information loss, $KTln2$ Joules of energy is wasted.

Here K denotes the Boltzman constant and T denotes the absolute temperature. Reversible computing is very much important in the field of quantum computing, bio-informatics, nanotechnology, optical computing, information security, dig- ital signal processing, low-power complementary metal oxide semiconductor (CMOS) design, deoxyribonucleic acid (DNA) computing, quantum-dot cellular automata etc. Reversible sorting circuit can play a crucial role in future computing devices as it can be used for improvement of operating system, networking areas. In this paper, two different algorithms have been proposed to sort 3 and 4 binary numbers. The whole process has been accomplished through the proposed comparators and switches. These circuits are designed with Fredkin and Toffoli gates which are reversible in nature.

This paper is organized as follows. Section II represents the background information on reversible logic. Section III represents the related works in this field. In Section IV, the proposed work has been discussed. Section V shows simulation of algorithms. The performance and cost analysis has been discussed in Section VI and the paper is concluded in Section VII.

PRELIMINARIES

This section represents the preliminary concepts of re- versible logic. The fundamental logic of reversibility, re- versible logic and some reversible logic gates related to our research work has been described here.

Sorting and Sorting Circuit

Sorting is any process that arranges items systematically, and has two common, yet distinct meaning of sorting is ordering: arranging items in a sequence ordered by some criterion. Sorting circuit is the circuit that can sort its inputs in ascending or descending order and an example is shown in Fig II-A.

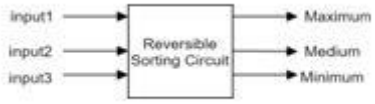

Fig1. *Block Diagram of Sorting Circuit*

Ancillary Input

The ancillary inputs are predefined input. It is also known as constant input. The number of ancillary input are minimized as much as possible in a reversible circuit.

Garbage Output

The unused output or the output which is not a primary input in the circuit is called the garbage output. Extra outputs can be added to make the number of inputs and outputs equal which is known as garbage output.

Quantum Cost

as the number of 1 1 or 2 2 primary reversible logic gates The Quantum Cost (QC) of a reversible circuit is defined that are needed to realize the circuit. The quantum gates are reversible and can manipulate qubits.

E.Delay

The number of gates in the critical path of a circuit is its delay [6]. The critical path is the the path from a primary input to a final output in the circuit with the maximum number of gates between them. F. Hardware Complexity It is denoted by aα + bβ + cγ where a b and c denotes the number of EX-OR, AND and NOT operations accordingly which are required to realize the circuit.

Related Work

There has not been any research work done yet on reversible sorting circuit to the best of our knowledge. But many researchers have worked on sorting from different angles at different times. Some previous works on sorting have been presented here. Canaan proposed a sorting algorithm and discussed existing algorithms.. Zhang worked on sorting-based IO connection assignment for flip-chip designs. Fuguo presented several incomplete sort algorithms for getting the median value. Molic demonstrated sorting algorithms on mobile platforms. A sorting unit based on FPGA Collaborative Hardware for Embedded Data Processing System was proposed by Z. Long and Z. Zhang .P. C. Petrut, A. Amaricai and O. Boncalo presented FPGA architecture for hardware-software merge sort . J. Madrenas, D. Fernndez and J. Cosp presented a lowvoltage current sorting circuit based on 4-T min-max CMOS switch . A. Rjabov proposed a Hardware-based systems for partial sorting of streaming data . X. Huang, X. Fan, S. Zhang and F. Zhanga proposed a tag sorting circuit in WFQ scheduler based . But none have proposed or designed a reversible sorting circuit. So this research is a unique one and can be explored much more.

Proposed Work

In this section, the components needed for comparing and constructing the reversible sorting circuit are discussed. The first component is proposed comparator circuit which compares two inputs of 3 bits. The second component is 2 : 2 switch which is needed for producing output bits according to the proposed comparator's output. A. Proposed Reversible Comparator Circuit

Comparator Circuit is a Circuit that can Compare Inputs

This logic unit will compare two binary numbers each of 3 bit length and will give the decision bit of which one is greater between them. Output, O = 0 means A>B and Output, O = 1 means A <B and means Don't care. The figure represents the reversible comparator circuit. The table 1:

TableI. *Truth Table For Proposed Reversible Comparator Circuit*

A_2	A_1	A_0	B_2	B_1	B_0	O
0	0	0	0	0	0	x
0	0	0	0	0	1	1
0	0	0	0	1	0	1
0	0	0	0	1	1	1
0	0	0	1	0	0	1
0	0	0	1	0	1	1
0	0	0	1	1	0	1

0	0	0	1	1	1	1
..	..	..	..	..	..	..
1	1	1	0	0	0	0
1	1	1	0	0	1	0
1	1	1	0	1	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0
1	1	1	1	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	1	x

TableII. *Truth Table For Proposed 2 : 2 Switch*

A	B	O	S_1	S_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

Generated based on two 3-bits binary numbers. Using this truth table and after simplifying , the expression is:

O =A 0 2B2 + A 0 2B 0 2B1 + A 0 1B2B0 + A 0 2A 0 1A 0 0+ A 0 2A 0 0B0 + A 0 1A 0 0B2 + A 0 0B2B0 (1)

B. Proposed Reversible 2 : 2 switch A 2 : 2 switch has been proposed in this section where Fredkin gate has been used. According to the comparator's output O the switch generates output bits. Figure 3 shows the proposed 2 : 2 switch and Table II shows the functionality of the switch. For Fredkin gate to perform 2 : 2 switch conversion we need to make O the decision bit from comparator the first input, second is A and third is B. Let O = 0 and target outputs are S1 and S2 can be obtained by the following equations.

S1 = O 0 A ⊕ OB = 1A ⊕ 0B = A (2)

S2 = O 0 A ⊕ OB = 0A ⊕ 1B = B (3)

According to equation 2 and 3 the 2 : 2 switch passes first input as S1 = A and second input as S2 = B if S = 0. If the selection bit S = 1 then it passes first input as S2 = A and second input as S1 = B. Selection bit O generated from the comparator.

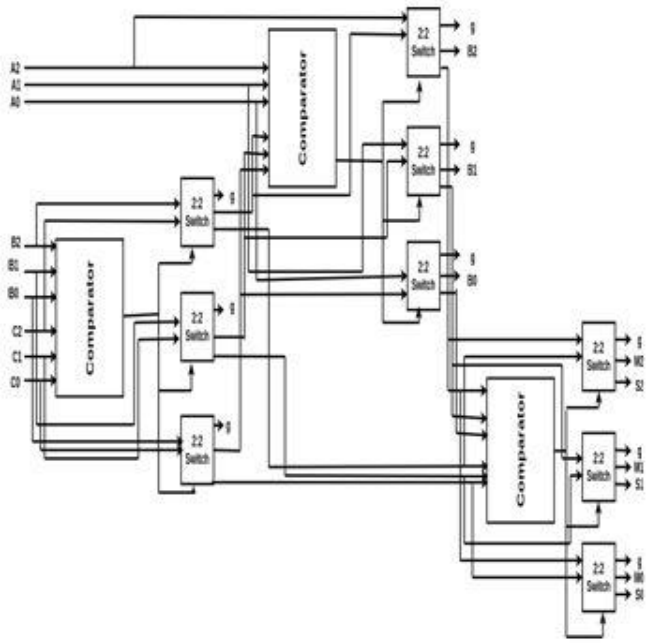

Fig4. *Reversible Sorting Circuit For Three 3-bit Binary Numbers*

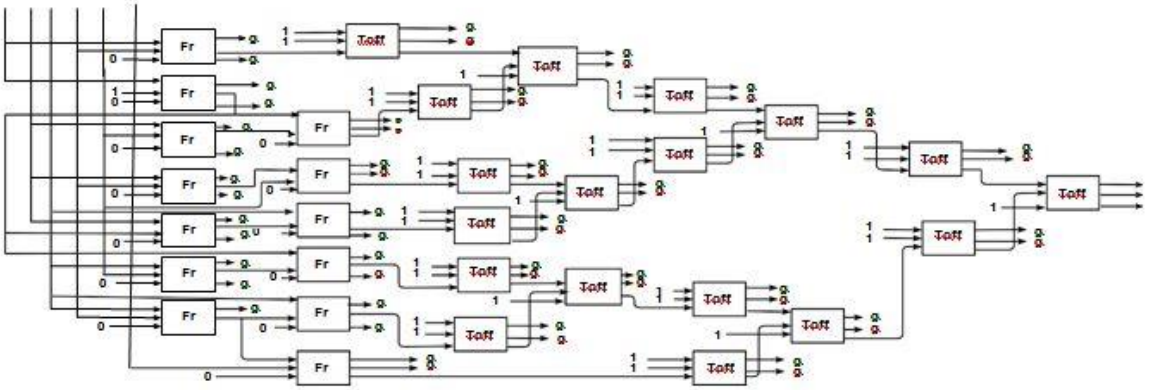

Fig2. *Proposed reversible comparator*

Reversible Sorting Circuit

The task of proposed reversible sorting circuits is to simply sort three or four binary numbers of 3-bit. To do this job, the reversible comparator is used for comparing the inputs. Proposed 2 : 2 switch will be used for transferring inputs into outputs based on the decision of comparator. According to Figure 4 the three inputs are A2A1A0, B2B1B0, C2C1C0.The inputs are sent to the comparators. According to the comparator's output bit the switch generates the output and the whole circuit follows the Algorithm 1. Finally the biggest output (B2B1B0), medium output (M2M1M0) and the smallest output (S2S1S0) is obtained in descending order. According to Figure 5 the four inputs are A2A1A0, B2B1B0, C2C1C0, D2D1D0. The whole circuit follows the Algorithm 2. Finally the biggest output (B2B1B0), greater medium output (M12M11M10), smaller medium output (M02M01M00) and the smallest output (S2S1S0) are obtained in descending order.

Simulation Of Algorithms

The two proposed algorithms have been simulated and tested with the help of DSCH3. DSCH3 simulator is used for verifying logic circuits output before the physical hardware design is implemented. It provides timing diagrams with input and output. Figure 6 shows the last three switches for algorithm 1 and Figure 7 shows the last three switches for Algorithm 2, which are included to verify the results. A. Simulation of Algorithm 1 (3 binary numbers) Let's assume the 3 inputs are X = 001, Y = 110, Z = 100

1) First comparator compares Y and Z and gives output, O0 = 0, Constant input C0=0 and C1=1

2) First three 2 : 2 switch gets Y and Z and O0 = 0 as input and passes G0 = 110 and S0 = 100 as output 3) Second comparator compares X and G0 and gives output, O1 = 1

4) Second three 2 : 2 switch gets X and G0 and O1 = 0 as input and passes B = 110 and S1 = 001 as output

5) Last comparator compares S1 and S0 and gives output, O2 = 1

6) Last three 2 : 2 switch gets S1 and S0 and O2 = 1 as input and passes M = 100 and S = 001 as output

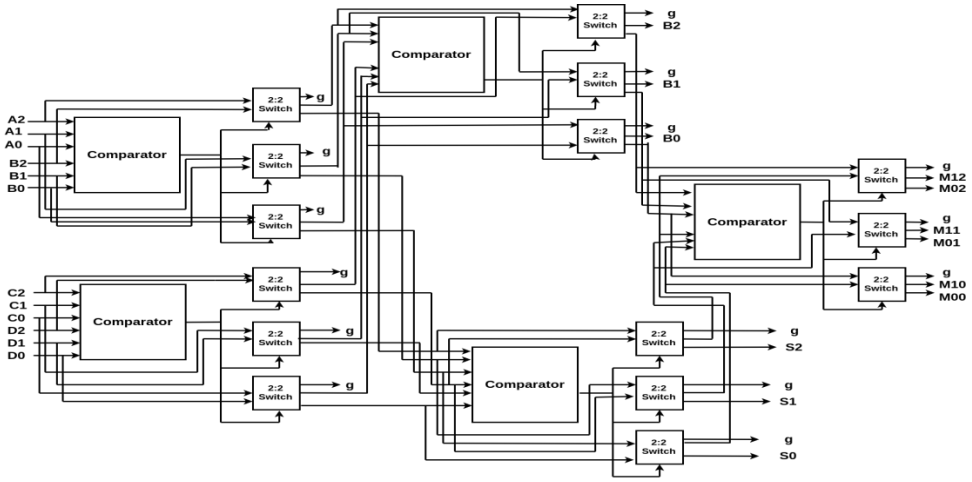

Fig5. *Reversible Sorting Circuit for Four 3-bit Binary Numbers*

Algorithm 1: Proposed algorithm to sort three binary numbers each of 3 bits Result

Result: Sorted numbers {B2B1B0 , M2M1M0 & S2S1S0}

Data: Data{A2A1A0,B2B1B0 & C2C1C0}

1 Apply Comparator where Input:={B2B1B0 & C2C1C0}; Output:={O0};

2Apply 2:2 switches where Input:= {B2B1B0,C2C1C0 & O0} and pass the greater one as G02G01G00 and the smaller one as S02S01S00, Output:={G02G01G00 & S02S01S00};

3Apply Comparator where Input:={G02 G01G00 & A2A1A0} Output:={S1}

4 Apply 2:2 switches where Input:={G02 G01G00,A2A1A0 & S1} and pass the greater one as B2B1B0 and the smaller one as S12S11S10, Output:={B2B1B0 & S12S11S10}

5Apply Comparator where Input:={S02S 01S00 & S12S11S10}; Output:={S2}

6 Apply 2:2 switches where Input:={S02 S01S00,S12S11S10 & S2} and pass the greater one as M2M1M0 and the smaller one as S2S1S0, Output:={M2M1M0 & S2S1S0}

Simulation of Algorithm 2 (4 binary numbers)

Let's assume the 4 inputs are W = 100,X = 001, Y = 000, Z = 010

1) First comparator compares W and X and gives output, O0 = 0, Constant input C0=0 and C1=1

2) First three 2 : 2 switch gets W and X and O0 = 0 as input and passes G0 = 100 and S0 = 001 as output

3) Second comparator compares Y and Z and gives output, O1 = 1

4) Second three 2 : 2 switch gets Y and Z and O1 = 0 as input and passes G1 = 010 and S1 = 000 as output

5) Third comparator compares G0 and G1 and gives output, O2 = 0

6) Third three 2 : 2 switch gets G0 and G1 and O2 = 1 as input and passes B = 100 and T0 = 010 as output

7) Fourth comparator compares S0 and S1 and gives output, O3 = 0

8) Fourth three 2 : 2 switch gets S0 and S1 and O3 = 0 as input and passes T1 = 001 and S = 000 as output

9) Fifth comparator compares T0 and T1 and gives output, O4 = 0

10) Fifth three 2 : 2 switch gets T0 and T1 and O4 = 0 as input and passes M1 = 010 and M0 = 001 as output

Performance and Cost Analysis

The performance and cost of the proposed circuits depend on various parameters. They are measured with number of reversible gates needed, hardware complexity, garbage outputs, quantum cost and critical path delay. A comparator circuit consists of 13 Fredkin gates and 18 Toffoli gates

Quantum cost of both Fredkin gate and Toffoli gate is 5. Fredkin gate has three inputs and three output. If the inputs are A, B and C then the output will be A, A0B⊕AC and A0C⊕ AB. Using Boolean algebra the two outputs can be written as A0B ⊕ AC = A0B + AC and A0C ⊕ AB = A0C + AB. For

Algorithm 2: Proposed algorithm to sort four binary numbers each of 3 bits

Result: Sorted numbers {B2B1B0,M12 M11M10,M02M01M00 & S2S1S0}

Data: {A2A1A0,B2B1B0,C2C1C0 & D2 D1D0}

1 Apply comparator where Input:={A2A1A0 & B2B1B0}; Output:={O0}

2Apply 2:2 switches where Input:= {A2A 1A0,B2B1B0 & O0}; and pass the greater one as G02G01G00 and the smaller one as S02S01S00, Output:={G02G01G00 & S02 S01S00} ;

3 Apply comparator where Input:={C2C1C0 & D2D1D0}; Output:={S1}

4Apply 2:2 switches where Input:= {C2C1C0,D2D1D0 & S1}; and pass the greater one as G12G11G10 and the smaller one as S12S11S10, Output:={G12G11G10 & S12S11S10}

5Apply comparator where Input:= {G02G01G00 & G12G11G10}; Output:={S2}
6Apply 2:2 switches where Input:= {G02G01G00,G12G11G10 & S2}; and pass the greater one as B2B1B0 and the smaller one as T12T11T10, Output:={B2B1B0 & T12T11T10}

7 Apply comparator where Input:= {S02S

01S00 & S12S11S10}; Output:={O3}

8 Apply 2:2 switches where Input:= {S02S 01S00,S12S11S10 & O3}; and pass the greater one as T02T01T00 and the smaller one as S2S1S0, Output:={T02T01T00 & S2S1S0}

9 Apply comparator where Input:= {T02T 01T00 & T12T11T10}; Output:={O4}

10 Apply 2:2 switches where Input:= {T02 T01T00,T12T11T10 & O4}; and pass the greater one as M12M11M10 and the smaller one as M02M01M00, Output:={M12M11M10 & M02M01M00} these two outputs, 2 NOT gates, 4 AND gates of 2 inputs and 2 OR gates of 2 inputs are needed. Transistor count for NOT gate is 1 and 2 inputs AND gate and OR gaate is 3 . So for a Fredkin gate transistor count is 2×1+4×3+2×3 = 20.

Toffoli gate has three inputs and three output. If the inputs are A, B and C then the output will be A, B and AB $\oplus$ C. Using Boolean algebra the third outputs can be written as AB $\oplus$ C = ABC0 + (AB) 0C. For the third output total 1 NOT gate, 3 AND gates of 2 inputs, 1 NOR gate of 2 inputs and 1 OR gate of 2 inputs are needed. Transistor count for NOR gate of 2 inputs is 2 . So for a Toffoli gate transistor count is 1 + 3 × 3 + 2 + 3 = 15.

The hardware complexity of Fredkin gate is 2α + 4β + 2γ and Toffoli gate is α +β.

The delay of both Fredkin and Toffoli gate is 5Δ. In a reversible comparator circuit the critical path contains 8 gates. So the total delay of comparator is 8×5Δ = 40Δ. In reversible sorting circuits the critical path is same and it contains 2

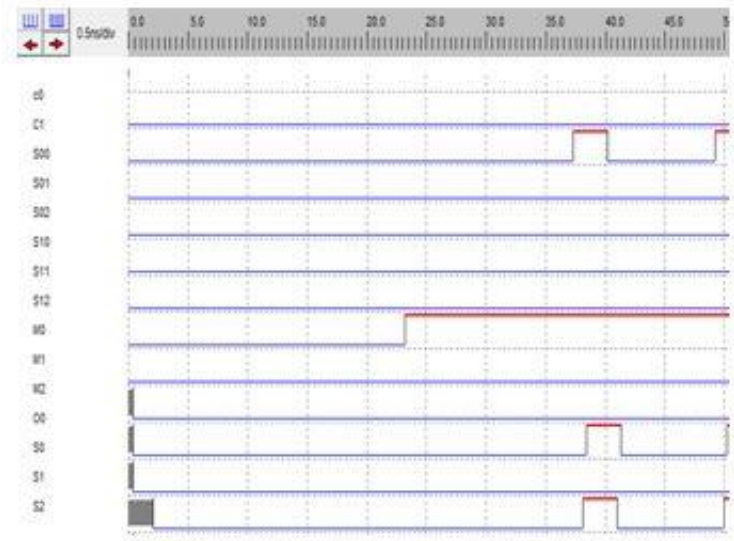

Fig.6. *Timing diagram of the Last Three 2 : 2 Switches for Three Binary Numbers*

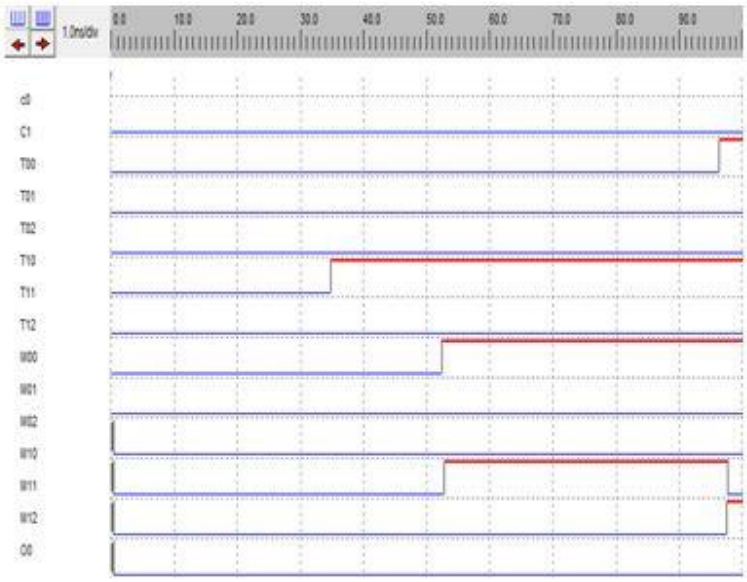

Fig7. *Timing Diagram of the Last Three 2 : 2 switches for Four Binary Numbers*

reversible comparators and 2 proposed 2 : 2 switches. As the proposed 2 : 2 switch is actually derived from a Fredkin gate, so it has delay of 5δ.

So the critical path delay for both circuits = 40Δ + 5Δ + 40Δ + 5Δ + 40Δ + 5Δ = 135Δ

Performance & Cost Analysis for 3 Binary Numbers

According to the figure 4 of proposed reversible sorting circuit for 3 binary numbers of 3-bit, it needs 3 comparators (each of them produces 2 garbage outputs) and 9 Fredkin gates as 2 : 2 switch (each of them produce 1 garbage output). So, the number of reversible gates=(13 + 18) × 3 + 9 = 102

Quantum cost=102 × 5 = 510

Garbage output=93 × 2 + 9 × 1 = 195

Proposed reversible sorting circuit needs 48 Fredkin gates and 54 Toffoli gates. So, the total transistor count = 48×20+54× 15 = 1770, which is shown in Table III.

Table III. *Cost Analysis Of Reversible Sorting Circuit For Three 3-Bit Binary Numbers*

Stage	Name of Reversible Gate	Number of Gate	Hardware Complexity
1	Fredkin Toffoli	13 18	13(2α + 4β + 2γ) 18(α +β)
2	Fredkin	3	3(2α + 4β + 2γ)
3	Fredkin Toffoli	13 18	13(2α + 4β + 2γ) 18(α +β)
4	Fedkin	3	3(2α + 4β + 2γ)
5	Fredkin Toffoli	13 18	13(2α + 4β + 2γ) 18(α +β)
6	Fedkin	3	3(2α + 4β + 2γ)
Overall	Fredkin Toffoli	48 54	48(2α + 4β + 2γ) 54(α +β)
Total	102	150α + 246β + 96γ	

Table IV. Cost Analysis Of Reversible Sorting Circuit For Four 3bit Binary Numbers

Stage	Name of Reversible Gate	Number of Gate	Hardware Complexity
1	Fredkin Toffoli	13x2 = 26 18x2 = 36	26(2α + 4β + 2γ) 36(α +β)
2	Fedkin	6	6(2α + 4β + 2γ)
3	Fredkin Toffoli	13x2 = 26 18x2 = 36	26(2α + 4β + 2γ) 36(α +β)
4	Fedkin	6	6(2α + 4β + 2γ)
5	Fredkin Toffoli	13 18	13(2α + 4β + 2γ) 18(α +β)
6	Fedkin	3	3(2α + 4β + 2γ)
Overall	Fredkin Toffoli	80 90	80(2α + 4β + 2γ) 90(α +β)
Total	170	250α + 410β + 160γ	

Performance & Cost Analysis for 4 Binary Numbers

According to the Figure 5 of proposed reversible sorting circuit for 4 binary numbers of 3-bit, it needs 5 comparators and 15 Fredkin gate as 2 : 2 switch. All of them produce 1 garbage output

So, the number of reversible gates=(13 + 18) × 5 + 15 = 170

Quantum cost=170 × 5 = 850

Garbage output=155 × 2 + 15 × 1 = 325

Proposed reversible sorting circuit for 4 numbers needs 80 Fredkin gates and 90 Toffoli gates. So, total transistor count = 80 × 20 + 90 × 15 = 2950, which is shown in Table IV

CONCLUSION

In this paper, two unique and efficient reversible sorting circuits are proposed which can sort three and four binary numbers each of 3-bit in descending order. Fredkin and Toffoli gates are used to make the circuit reversible. Reversible comparator and the proposed 2 : 2 switch are used for sorting binary bits. This circuit is a fundamental work in the field of reversible sorting circuit which has minimum quantum cost. The circuit is optimized in terms of quantum metrics. In the future, the design can be broadened to sort more than 4 numbers. The comparator can also be changed internally to sort numbers of 4-bit sized or bigger sized. The two proposed reversible sorting circuits can be used for efficient lookup or search and structured processing of data.

REFERENCES

[1] R. Landauer, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 44, no. 1/2, p. 261, 2000.

[2] M. U. Haque, Z. T. Sworna, and H. M. H. Babu, "An improved design of a reversible fault tolerant lut-based fpga," in 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), pp. 445–450, IEEE, 2016.

[3] K. Datta, V. Shrivastav, I. Sengupta, and H. Rahaman, "Reversible logic implementation of aes algorithm," in 2013 8th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS), pp. 140–144, IEEE, 2013.

[4] ".Transistor count." https://e lectronics.Stack exchange.com/questions/ 99722/and-or-gates-3-transistors-nand-nor-gates-2-transistors-why. Last Accessed on : September 2,2018.

[5] R. Wille and R. Drechsler, "Bdd-based synthesis of reversible logic for large functions," in Proceedings of the 46th Annual Design Automation Conference, pp. 270–275, ACM, 2009.

[6] M. S. Al Mamun, I. Mandal, and M. Hasanuzzaman, "Design of universal shift register using reversible logic," International Journal of Engineering and Technology, vol. 2, no. 9, pp. 1620–1625, 2012.

[7] P. C. Petrut, A. Amaricai, and O. Boncalo, "Configurable fpga architecture for hardware-software merge sorting," in 2016 MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems, pp. 179–182, June 2016.

[8] R. Zhang, X. Wei, and T. Watanabe, "A sorting-based io connection assignment for flip-chip designs," pp. 1–4, Oct 2013.

[9] D. Fuguo, "Several incomplete sort algorithms for getting the median value," Int. J. Digital Content Technol. Appl., vol. 4, no. 8, pp. 193–198, 2010.

[10] R. Meolic, "Demonstration of sorting algorithms on mobile platforms," in CSEDU, pp. 136–141, 2013.

[11] C. Canaan, M. Garai, and M. Daya, "Popular sorting algorithms," World Applied Programming, vol. 1, no. 1, pp. 42–50, 2011.

[12] J. Madrenas, D. Fernndez, and J. Cosp, "A low-voltage current sorting circuit based on 4-t min-max cmos switch," in 2010 17th IEEE International Conference on Electronics, Circuits and Systems, pp. 351–354, Dec 2010.

[13] A. Rjabov, "Hardware-based systems for partial sorting of streaming data," in 2016 15th Biennial Baltic Electronics Conference (BEC), pp. 59–62, IEEE, 2016.

[14] X. Huang, X. Fan, S. Zhang, and F. Zhang, "An optimized tag sorting circuit in wfq scheduler based on leading zero counting," in 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Techno logy, pp. 533–535, Nov 2010.

[15] "Kmap simulator." http://www.32x8.com. Last Accessed on : July 26,2018.

[16] "Sorting defination." https://en.wikipedia. org/wiki/Sorting. Last Accessed on : Decem ber 26,2018

Citation: *Balasani Naga Nandini et al, "Capable Design of a Reversible Categorization Circuit", International Journal of Research Studies in Science, Engineering and Technology. 2019; 6(2): 40-47. https://doi.org/ 10.22259/2349-476X.0602006*