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Time Interleaved Parallel ADC with Efficient Decoder and Improved Sampling Switch

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Abstract: *Buffered multiplexer based decoder are proposed in the literature for high speed parallel ADCs with low power and less hardware requirements.The parallel ADC designed by using voltage controlled amplifier (VCA), bootstrap switch, a comparator array consists of 63 comparators, D filp-folp's and buffered mux based decoder. A buffered mux based decoder compares with the folded decoder with respect hardware, power consumption and critical path.Bootstrapped switches is used to migrate the problem with varying on-resistance and poor conduction.The buffered mux based decoder is used to converts 63-bit thermometer code into 6-bit binary code.The parallel ADC integrated on chip micro controller calibration, it is used for watchdog and it compensate the nominal non linearity of the fine VCA.The parallel ADC with 0.9 supply,400mv of full scale voltage at 2.5-GSamples/second consumes 15-28mW of power approximately in 130nm cmos technology.*

Keywords: *10G Ethernet, bootstrap switch, folded decoder, A/D convertors, buffered mux based decoder, Metastability errors, critical path.*

1. INTRODUCTION

The most of signals in the real world are analog (continuous in amplitude and time). In order to produce the digital signal, the analog signals are converted into the digital form by using a circuit called analog-to-digital converter. The usage of 10G Ethernet is extremely increased to amuse the demand for higher bandwidth. This paper implements a 6 bit parallel A/D Converters with 2.5-GS/s which can be used in the way of 4 times interleaved parallel architecture for 10GE functionalities. This parallel ADC design facilitates lower predicted metastability errors, flexibility, low hardware design than remaining high speed low to medium resolution ADC's. The basic diagram of time interleaved parallel adc is shown in the figure.1.It is implemented in 130nm CMOS technology. The ADC characterized in this document is used for the 4way interleaved runs at 10GSample/s for DSP based receiver that could be used the NRZ 10GE standards. This paper targets on the design of bootstrap switch and implementation of buffered decoder for the ADC and on comparative analysis of folded decoder and buffered multiplexer decoder implementations. In addition, owing to the nature of successive bit decoding, momentous time interleaving may be unavoidable to ensure better metastability error rate, which is one of major requirement in such applications.

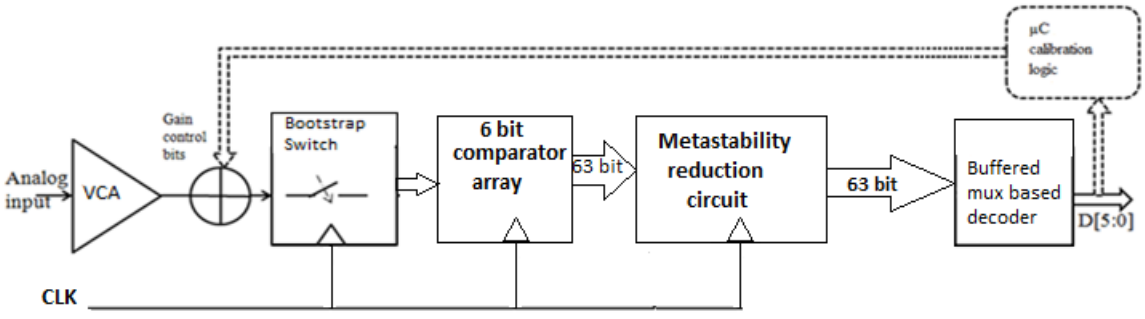


Figure1. *Top level of parallel ADC*

2. CIRCUIT IMPLEMENTATION

2.1. Voltage-Controlled Amplifier (VCA)

The VCA adjust the input signal to provide a swing approximately 400 mV differential peak-to-peak to the bootstrap switch. Fig. 2 shows the circuit of the source degenerated differential amplifier

equipped with VCA. The purpose of source degeneration is to improve the linearity of the amplification. The source degeneration utilizes a linear resistor at the source terminal as shown in figure 2. This resistor reduces the swing at the gate to source, making the input/output characteristics more linear.Over all transconductance of the source degenerative amplifier is

$$Gm = gm / (1+ gm*Rs).$$

Where Rs is equivalent source resistance of resistor network.

The M3and M4 is used to extending bandwidth during normal operation also detach the input signal from the load during calibration. Charge feedback through the gate-to-drain overlap capacitance of M1 and M2 can disturb circuit functionality. A Cross-coupled device M3 and M4 implements the first-order cancellation of this effect.

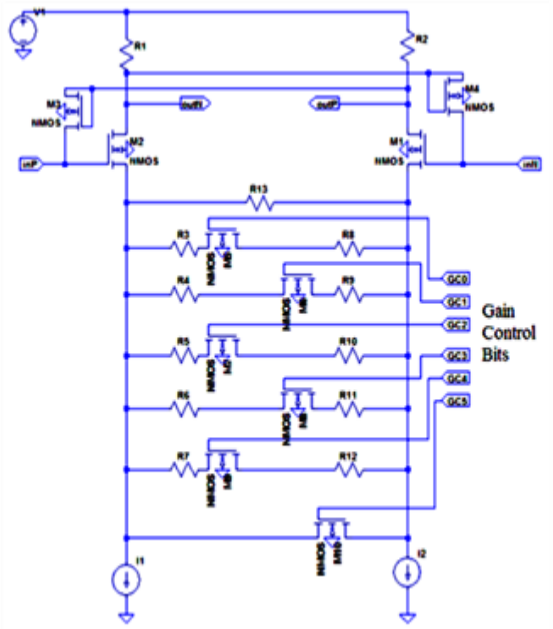


Figure2. *Source-degenerated variable controlled amplifier (G)*

2.2. Bootstrap Switch

A bootstrapped switch is a design technique to migrate the problem with varying on-resistance and poor conduction. These switches are realized with a one pass transistor and supplementary devices for generation of gate-source voltages for the pass transistor.When the off-state the gate is aligned to ground and the transistor is in cut-off region.The main difference between the regular analog switches and bootstrapped switch is present in the on-state, where the gate to channel voltage is kept constant. It is done by connecting a constant offset voltage between the source and gate terminals of the main switch. This voltage could be obtained by the using of a capacitor pre-charged in the off-state. Depending upon the information signal, this offset will reach voltages equal to Vdd .Considering the complete voltage at the gate terminal exceeds the supply voltage, mentioned switches have to be designed correctly to prevent they don't violate all reliability constraints.

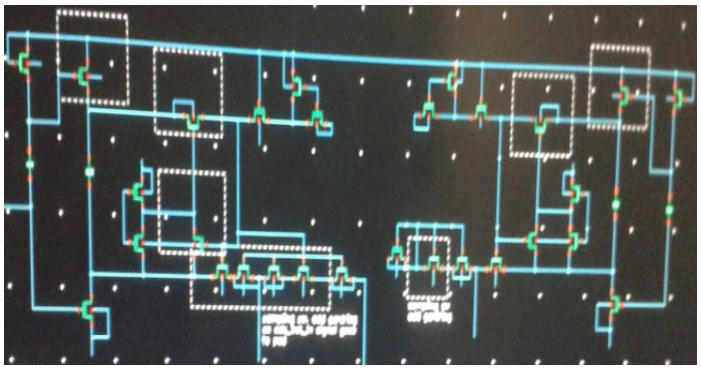


Figure3.*Bootstrap switch*

2.3. Dynamic Comparator

Dynamic comparator uses dual input and single output differential amplifier as latch stage suitable for high speed ADC with low power dissipation, high speed and high immune to noise. The comparator array consists of resistor ladder and 63 active comparators .The ladder range is 400 mVdpp, resulting in a nominal LSB value of 6.25 mV. In order to achieve a power efficient design, the dynamic comparator in this ADC doesn't contain any pre-amplifiers. In clock tree, local clock buffer is provided for each comparator and that can be deactivated during individual comparator power down to save the power.

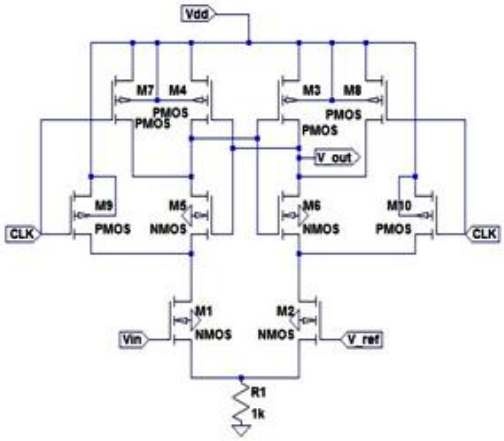


Figure3. *Dynamic comparator*

Fig. 3 shows the design of the dynamic comparator, which is based on a dynamic-sense amplifier latch incorporating several modifications. The comparator compares the output of bootstrap switch sampled input signal with the reference generated by the resistor ladder. A voltage of 400 mVdpp is provided to the resister ladder as full-scale voltage of parallel ADC. Comparison is performed by differential amplifier pair M1–M2. The output of a dynamic comparator is HIGH whenever sampled input voltage is larger than the reference voltage generated by ladder at the another input of the comparator, otherwise the output is inverted clock since the comparator is working in dual input and single output mode the inverted clock region will be cancelled and considered as LOW. The output of comparator array is 63 bit thermometer code. To prevent Metastability-related error propagation, the thermometer code goes through a sequence of flip-flops before arriving at the decoder inputs.

2.4. Decoders

2.4.1. Folded Wallace Tree Decoder

In the parallel ADC, the purpose is to reduce the amount of hardware by using the same comparator for different reference voltages. The dimensions of the Wallace tree and the delay is depending on the number of bits that will be added, i.e. the width of the base of the tree. An idea is to split the output of the comparators into2^k different intervals. They were multiplexed to a single Wallace tree decoder, which can be reduced in size compared with the full one in. A full adder might be constructed from three 2:1 multiplexers with two multiplexers in the critical path. so, according to the number of 2:1 multiplexers needed (Y_N) and the critical path (C_N) for the folded decoder is

$$y_N = 3 \cdot \left(\sum_{i=1}^{N-k} (i-1) \cdot 2^{(N-k-i)} \right) + 2^N - 2^{N-k} \quad (1)$$

$$c_N = 4N - 3k - 6, \quad (2)$$

respectively. Each C_N is equal to the propagation delay of a 2-input ex-or gate (t_{xor}) which can similar to the propagation delay of a 2:1 multiplexer ($t_{Mux)}$.

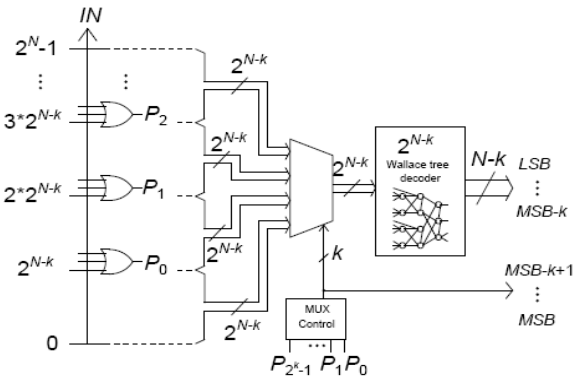


Figure4. *Folded Wallace tree decoder*

2.4.2. Buffered Multiplexed Based Decoder

The 2x1 inverted multiplexer is shown in the figure5.The output of pass transistor is connected to odd number of inverters in order to provide stronger signal. This segment will first illuminate the idea behind the presented buffered multiplexer based decoder and second describe how it will be generalized. For an N-bit parallel ADC the most significant bit (MSB) of the binary output is high if more than half of the outputs in the thermometer scale are logic one. So most significant bit (MSB) is the same as the thermometer output at 2^{N-1} level. To find the value of the second most significant bit (MSB-1) the original thermometer scale is prorated into partial thermometer scales, separated by the output at 2^{N-1} level as depicted as the flow diagram in Figure 7.

The partial thermometer scale to decode is chosen by a set of inverted 2:1 multiplexers, where the preceding decoded binary output is connected as the control input of the inverted multiplexers.MSB-1 is then determined from the selected partial thermometer scale in the likewise as MSB initiated from the full thermometer scale. The preferred scale is thereby the scale that consists of the information about MSB-1, i.e. the lower partial thermometer scale if the output at level is logic zero or else the upper partial thermometer scale is used.

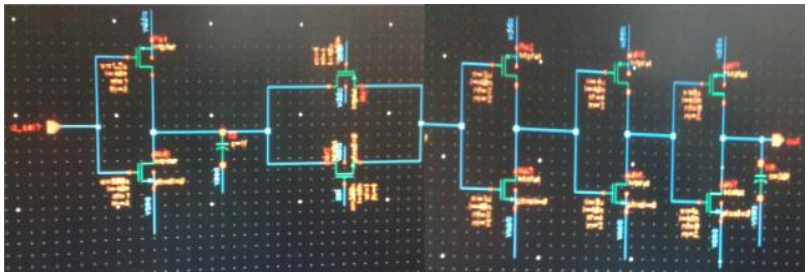


Figure5. *Inverted 2x1 mux*

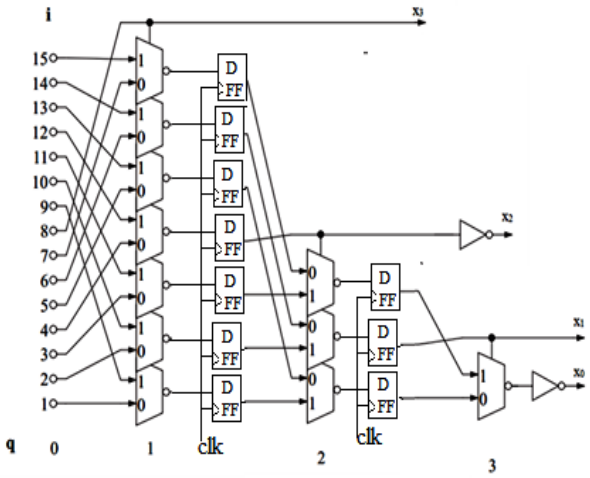


Figure6. *Buffered mux based decoder for 4 bit decoder*

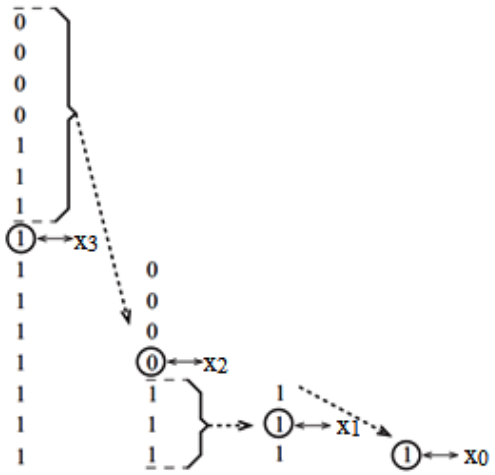


Figure7. *Flow of buffered multiplexer based decoding*

The buffered based decoder for 4 bit decoder is shown in figuer6.It is continued recursively until only one 2:1 multiplexer remains. Its output is the LSB of the binary output. Due to the regular design of this decoder it can easily be widen to function in a system of higher resolution than 4 bits, which is explained further below. The regular design should also be help in the physical layout. The outputs x_q of the decoder is the equivalent binary value of the thermometer code, where q=0,1,2,3,.....N-1. The column q=1 is the first multiplexer column. Hence the output $i_q = 2^{N-q-1}$ is fed to the control inputs of the multiplexers in q+1 column. This is also the output of the x_{N-q-1} decoder, where x_{N-1} is the MSB of the binary output. The output of the multiplexer in column q=*N*-1 is the LSB of the binary output, i.e.x_0.

In general, for an *N*-bit parallel ADC the thermometer output has 2^N - 1 levels ($i_{q=0}$). The thermometer output $i_{q=0}$ or multiplexer output $i_{q>0}$ is fed to the '0' ($i_q < 2^{N-q-1}$) or '1' ($i_q < 2^{N-q-1}$) input of the multiplexer of level i_q *modulo* 2^{N-q-1} and column q+1 ,where $i_{q = 1,2,3,4,.....}$ 2^{N-q}-1.So the presented decoder required number of 2:1 multiplexers Y_N and the critical path C_N in units of t_{MUX} can be formulated as:

$$Y_N = \sum_{i=1}^{N-1} [\, 2^{(N-i)} - 1] \quad (3)$$

$$C_N = N - 1 \quad (4)$$

3. COMPARISON OF THE DECODERS

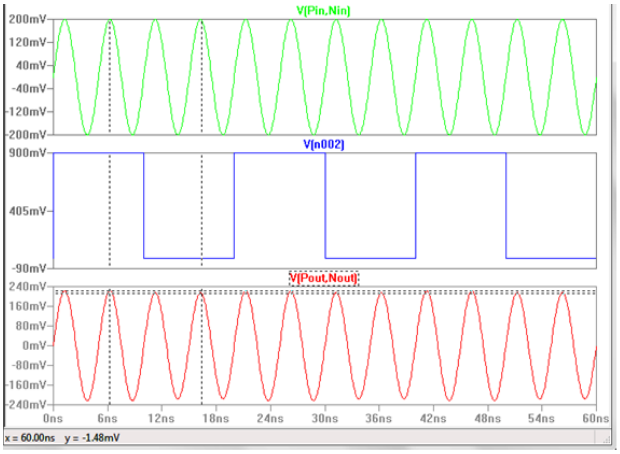
The buffered multiplexer based decoders have capable and promising properties in terms of amount of hardware and critical path. If instead an ones-counter is used as the decoder it concedes speed versus power trade-off not only by directly trading power for speed, but also in terms of selecting appropriate ones counter/adder topology. A comparison of the performance between the folded decoder and the buffered Mux based decoder is given in T able 1. The performance is considered in terms of amount of hardware and length of the critical path.

Table1. *Performance comparison of 6 bit parallel ADC*

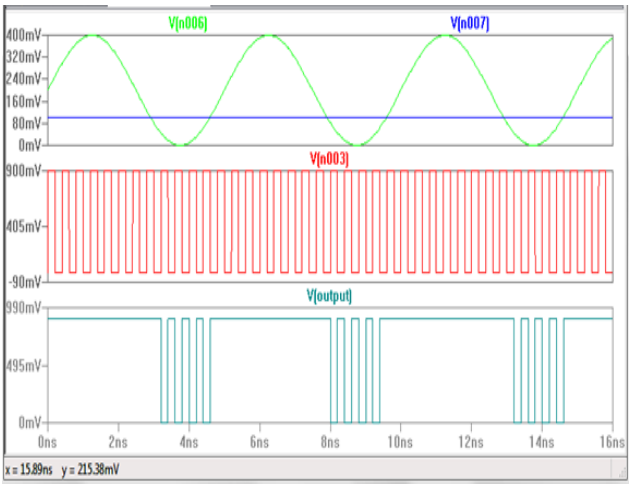
Type of Decoder	**N.of MUX's**	**Critical path**
Folded Decoder	81	12 t_{MUX}
Buffered MUX based Decoder	57	5 t_{MUX}

As seen in Table 1, the hardware is extremely reduced when using the buffered MUX based decoder. For the buffered MUX based decoder, the number of multiplexers is reduced by more than 30% compared to the folded decoder. This is likely to translate to a power saving. Table 1 also indicates that the suggested solution has the potential of being faster than the folded decoder, since its critical path is shorter. The metastability will be reduced by placing flip-flop between the muxes.

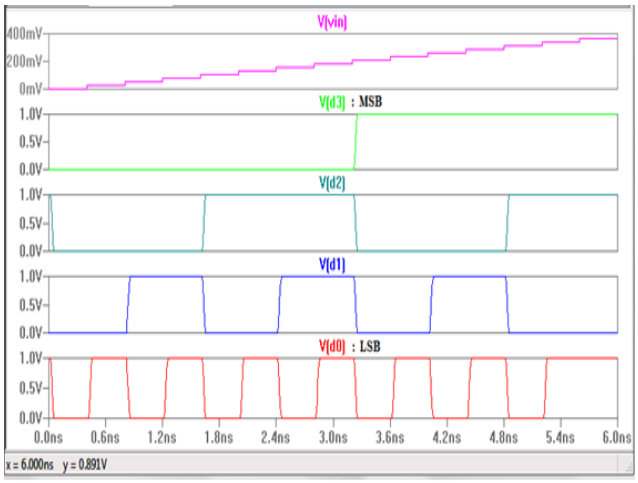
4. SIMULATION RESULTS



Figuer8. *Simulation of VCA*



Figuer9. *Simulation of dynamic comparator*



Figuer10. *Simulation of time interleaved parallel ADC*

5. CONCLUSION

We have presented a 2.5-GS/s,0.9V supply, 6-bit, 15- 28 mW, parallel ADC for a universal 10GE DSP-based receiver. Our study demonstrates that the bootstrap switch is for to minimize the on-resistance during track mode and also minimize sample-to-hold step size during hold mode. Buffered multiplexer based decoder is a pleasant approach for designing thermometer-to-binary decoder. The hardware used and area consumption is lesser than compared to the other exiting decoders and the critical path is briefer and it is useful for lower power applications. In addition, it is more traditional design than the other decoders, which can be added advantage when doing the layout.

REFERENCES

[1] Aida Varzaghani, "A 10.3-GS/s, 6-Bit Flash ADC for 10G Ethernet Applications" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 12, pp. 3038-3048, December 2013.

[2] Erik Sail, and mark Vesterbacka, "A MUL- TIPLEXER BASED DECODER FOR FLASH ANALOG-TODIGITAL CONVERTERS" IEEE, August, 2004.

[3] B. Hochet, and F. Kaess, "New Encoding Scheme For High-speed Flash ADC's", 1997 IEEE International Symposium on Circuits and Systems, pp. 5-8, June 9-12,1997, Hong Kong .

[4] K. Uyttenchove, A. Marque, "A 6-bit 1 GHz Acquisition Speed CMOS Flash ADC with Digital Error Correction",IEEE, pp. 249-252, CUSTOM INTEGRATEDCIRCUITS CONFERENCE, 2000.

[5] J. Terada, Y. Matsuya, and F. Morisawa, "8- mW, 1-V, 100-MSPS, 6-BIT A/D CONVERTER USING A TRANSCONDUCTANCE LATCHED COMPARATOR", pp.53-56, IEEE.

[6] M. F. Flynn et al, "Digital calibration incorporating redundancy of flash ADCs" ,IEEE Trans. Circuits Syst.II, vol. 50, no. 5, pp. 205–213,May 2003.

[7] Sunghyun Park, "A 4-GS/s 4-bit Flash ADC in 0.18-µm CMOS", In IEEE Journal of Solid-State Circuits,VOL.42, NO.9, pp. 1865-1872, September 2007.

[8] Hamid Reza Mafi, and Hossein Shamsi, "A 10-Bit 50-MS/s Charge Injection Pipelined ADC Using a Digital Calibration", IEEE, 9 th International Multi-Conference on systems, signals and Devices,2012.

[9] Vladimir Stojanovic, Chih-Kong Ken Yang, "A Serial-Link Transceiver Based on 8-GSamples/s A/D and D/A Converters in 0.25-µm CMOS"IEEE Journal of Solid-State circuits, vol. 36, NO. 11, November 2001.