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# Low Power Multiply Accumulate Unit (MAC) for DSP Applications

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**Abstract:** *Wireless Sensor Network (WSN) presents significant challenges for the application of distributed signal processing and distributed control. These systems will challenge us to apply appropriate techniques to construct capable processing units with sensing nodes considering energy constraints. Digital Signal Processing (DSP) is one of the capable processing units, but it is not commonly used in WSN because of the power constraint. The Multiply-Accumulate Unit (MAC) is the main computational kernel in DSP architectures. The MAC unit determines the power and the speed of the overall system; it always lies in the critical path. Developing high speed and low power MAC is crucial to use DSP in the future WSN. In this work, a fast and low power MAC Unit is proposed. The proposed architecture is based on examination of the critical delays and hardware complexities of merged MAC architectures to design a unit with a low critical path delay and low hardware complexity. The new architecture reduces the hardware complexity of the summation network, thus reduces the overall power. Increasing the speed of operation is achieved by feeding the bits of the accumulated operand into the summation tree before the final adder instead of going through the entire summation network.*

**Keywords:** *Digital Signal processing, Multiply-Accumulate Unit, Wireless Sensor Network.*

## 1. INTRODUCTION

WSNs are networks of compact micro sensors with wireless communication capability. These tiny devices are comparatively cheap with the potential to be distributed in large numbers. WSNs have many applications of data gathering range from the health care to the military. Architectural challenges such as energy consumption, computational power, communication channels, energy sources, and sensing ability are posed for designers. WSN can be seen as a special case of embedded system, which provides the computational platform for hardware and software components to interact with the environment and other nodes.

Each sensor node has a processing unit. Many different types of processing units can be integrated into a sensor node. There are a large number of commercially available microcontrollers, DSPs, and field programmable gate arrays (FPGAs), which allows a big flexibility for processing unit implementations. The sensor nodes available in the market depend on an 8-bit or 16-bit microcontroller. FPGA is not used in the current sensor nodes because its power consumption is not as low as sensor nodes should be. Moreover the FPGA is not compatible with traditional programming methodologies. Currently, DSP is being a challenge for node demanding, such as a gateway or a robust sensor node, which can be the head of hierarchical cluster in a wireless sensor network. The future WSN needs DSP for more computational capabilities in order to engage in signal processing operations of the complex applications.

Signal processing in wireless sensor network has a huge range of applications. Infinite Impulse Response filtering (IIR), Finite Impulse Response filtering (FIR), and Kalman Filter (KF) find applications in object tracking, environmental monitoring, surveillance, and many other applications. These tasks are very computationally intensive and they could easily strain the energy resources of any single computational node in a wireless sensor network. In other words, most sensor nodes do not have the computational resources to complete many of these signal-processing tasks repeatedly. Since MAC unit is the main computational kernel in DSP architectures. Therefore, saving power at the MAC unit level will have a significant impact on the energy consumption of each node. Consequently, energy efficient system extends the WSN's lifetime and increases its computational capabilities. In this work we propose a fast and low power MAC Unit.

This paper is organized as follows. Section 2 provides a brief background in the general construction of the MAC unit. Section 3 introduces the related work. Section 4 explains the merging architecture. Section V introduces the proposed architecture. The results are given in section 6. Section 7 concludes the work.

## 2. General Construction of MAC

The MAC operation is the main computational kernel in Digital Signal Processing (DSP) architectures. The MAC unit is considered as one of the fundamental operations in DSP and it becomes a basic component in Application-Specific-Integrated-Circuits (ASIC).

The MAC unit determines the speed of the overall system; it always lies in the critical path. Developing a high speed MAC is crucial for real time DSP applications. Moreover, with the ever-increasing demand for WSN, a MAC unit with low power consumption would surely lead the market. Many researchers have attempted in designing MAC architectures with high computational performance and low power consumption.

In order to improve the speed of the MAC unit, there are two major bottlenecks that need to be considered. The first one is the partial products reduction network that is used in the multiplication block and the second one is the accumulator. Both of these stages require the addition of large operands that involve long paths for carry propagation.

Multiply-Accumulate is a common operation that computes the product of two numbers and adds that product to an accumulator. The multiplier A and multiplicand B are assumed to have n bits each and the addend Z has (2n+1) bits.

$$Z \leftarrow (AxB) + Z$$

The MAC Unit is made up of a multiplier and an accumulator as shown in Fig. 1.

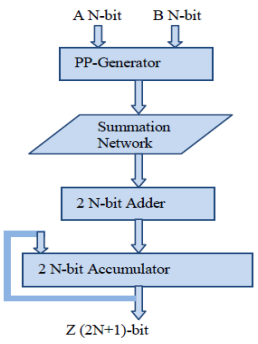



**Fig1.** *Basic Mac Unit*

The multiplier is divided into the partial products generator, summation network, and final adder. The summation network represents the core of the MAC unit; it reduces the number of partial products into two operands representing a sum and a carry. The summation network occupies most of the area and consumes most of the circuit area and delay. Several algorithms and architectures are proposed in an attempt to optimize the implementation of the summation network. The final adder is then used to generate the multiplication result out of these two operands. The accumulator is used to perform a double precision addition operation between the accumulated operand and multiplication result. Due to the large operand size, the accumulator required a very large adder.

## 3. THE MERGING ARCHITECTURE

The merged MAC architecture is based on fully utilizing the summation tree. Feeding the accumulated data bits into the unused inputs of the 4:2 compressors as shown in Fig. 2 can do this. This will save the cost of the additional accumulator by merging the accumulation (1) operation with the multiplication circuit. This can directly result in increasing the overall speed of the MAC operation. Power consumption and circuit area are saved as well.

The 8-bit MAC unit architecture is based on taking advantage of the free input lines of the available 4:2 compressors to implement the accumulation operation by feeding the bits of the accumulated operand into the summation tree, as shown in Fig. 3. The decision of where to insert the bit Z7 determines the number of required modified 4:2 compressors. The 8-bit MAC unit architecture consists of two compression stages. Stage one has two levels of compression. Each level has a combination of half adder, full adder and a modified 4:2 compressor [9].

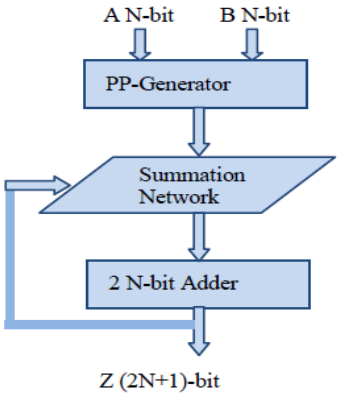



**Fig2.** *Merged Architecture*

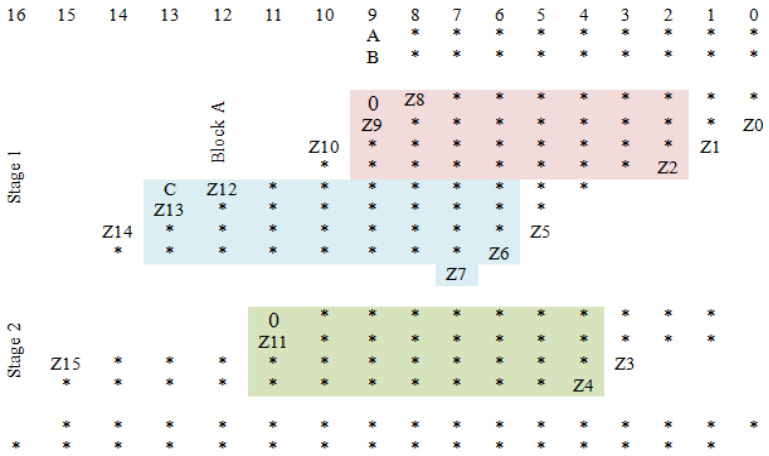



**Fig3.** *Data bit Distribution in the Merged MAC Unit*

The best place to insert this bit is in the 8th column in block "A" of the first stage and use a modified 4:2 compressor at this location to accommodate the extra bit [9]. The modified 4:2 compressor used will generate an additional carry out bit that is supposed to be fed to the next column. This in turn will require an additional modified 4:2 compressor in the 9th column at the first stage, which will also have an additional carry out.

## 4. PROPOSED ARCHITECTURE

The proposed MAC architecture is based on increasing the overall speed and throughput of the MAC and reducing the overall area of it. Saving the area is achieved by fully utilizing the compressors instead of putting zeros in free inputs. Increasing the speed is achieved by reducing the critical path by changing the MAC structure. The 32-bit MAC unit architecture is very large, so the 8-bit MAC unit architecture is used to explain the contribution and the 32-bit MAC unit can apply the same principle.

Fig. 4 shows the proposed distribution for an 8-bit MAC unit; the compression network consists of two stages. In the first stage, there are two compression levels A and B that are used to reduce the number of partial products from 8 to 4. The bits of the accumulated operand Z are inserted within the network, before the final adder in the second stage, in those empty locations at the corresponding columns such that those 4:2 compressors are fully utilized. The bits Z0, Z1, Z2, Z12, Z13, and Z14 inserted in the first stage, the bits Z3, Z4,

Z5, Z6, Z7, Z8, Z9, Z10, Z11, and Z15 are inserted in the second stage. The proposed structure reduces the number of compressors from 24 to 22 compressors. Two full adders are used instead of the saved two compressors. In the fifth column we used a modified compressor in stage 1 (block A), so we were capable of using a full adder in stage 2.We also use two modified compressors in the eighth, ninth and the eleventh column to save a compressor in the tenth column in stage 2 (block A), as shown in Figure 4.

The feedback of the critical path of Z8 output is done in the stage 2 to speed up the design, instead of feeding it in stage 1, so we save the time, which was consumed in stage 1. When the number of input bits increases the number of the stages in the summation network increases. The numbers of stages for 8-bit, 16-bit and 32- bit MAC unit are 2, 4 and 9 stages respectively. So the time saving will increase for 32-bit MAC unit, because it has many stages.

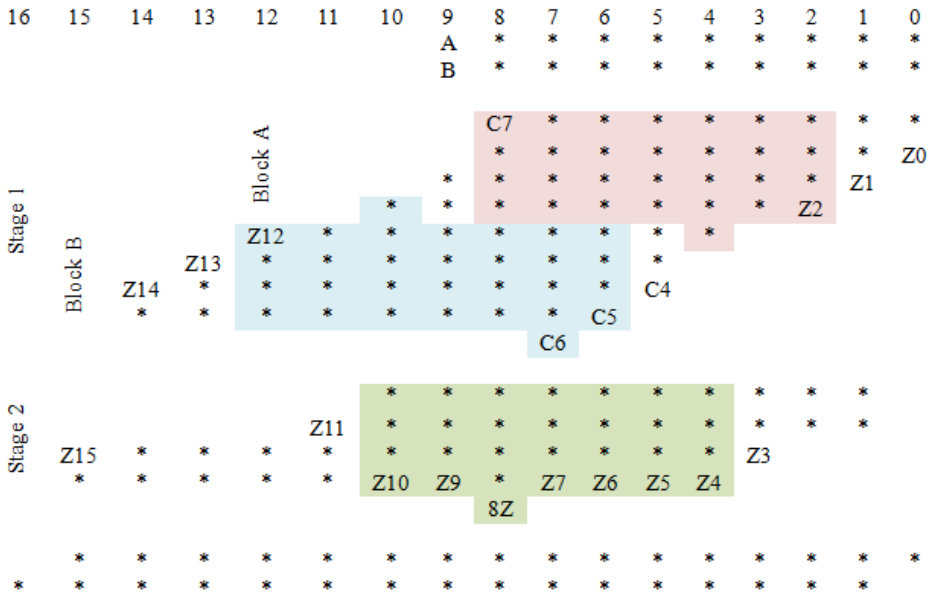
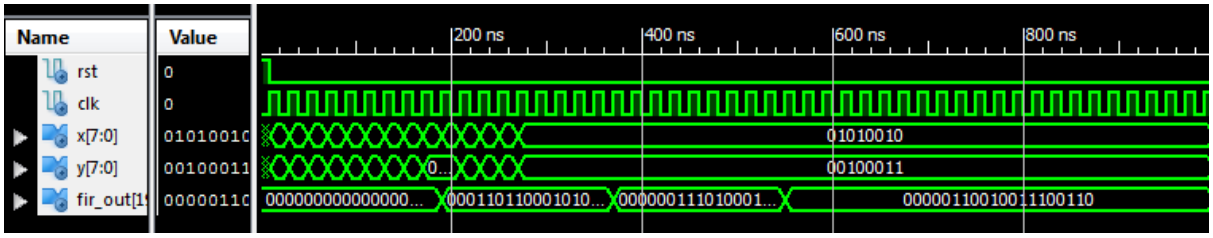


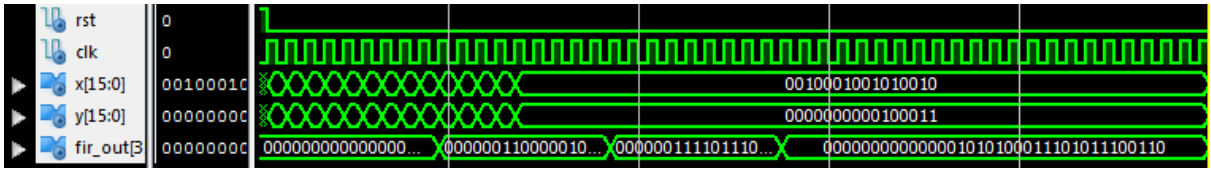

**Fig4.** *Data bit Distribution in the Proposed MAC Unit*

## 5. SIMULATION RESULTS

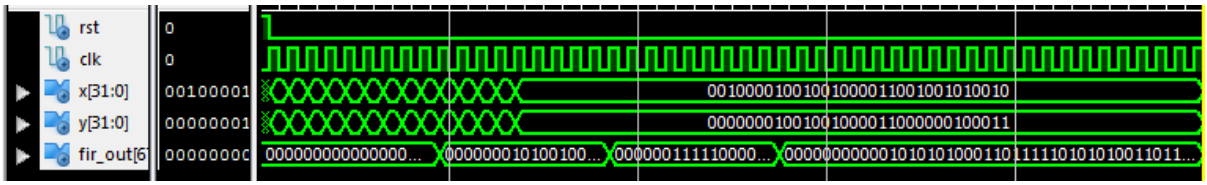
**Proposed_8bits**




**Proposed_16bits**




**Proposed_32bits**




## 6. CONCLUSION

In this paper we developed a fast and low power Multiply Accumulate (MAC) Unit. The proposed and the merged mac unit for 8bit, 16bit, and 32bit mac unit are implemented the number of the 4:2 compressors used for both the proposed MAC unit and merged mac unit. These saved compressors reduce the area of the proposed mac unit.

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