International Journal of Research Studies in Science, Engineering and Technology
Volume 2, Issue 7, July 2015, PP 37-44
ISSN 2349-4751 (Print) & ISSN 2349-476X (Online)

Fault Dictionary Based Single Hard Fault Detection in Non Linear Analog Circuits

G. Puvaneswari, S. Uma Maheswari

Department of Electronics and Communication Engineering,
Coimbatore Institute of Technology, Coimbatore, India

Abstract: *A method to detect single hard faults in non linear analog circuits based on fault dictionary is proposed. The method uses modified nodal analysis (MNA) to simulate and to derive the circuit parameters or diagnosis variables of the circuit under test (CUT). Test vectors which are used as fault dictionary are generated from the values and location of components of CUT. To solve the tolerance challenge in analog circuit testing, test vectors are generated for lower and upper bound values of components of CUT and also the diagnosis variables are measured. Test vectors are used to determine the suitable diagnosis variables for testing. A circuit is said to be fault free if the diagnosis variables are within the bound values. To identify the faulty conditions of the components, a fault variable corresponding to each component of CUT is estimated from the diagnosis variables and test vectors. A lowest value of fault variable indicates the faulty conditions of the components of CUT. The proposed approach is tested on bench mark circuits.*

Keywords: *analog circuits – fault dictionary –hard faults- modified nodal analysis – tolerance.*

1. INTRODUCTION

In testing of analog circuits, the factors like component tolerance and nonlinearity of components limit the development of standard models. Two fault models namely parametric or hard faults describe the faulty conditions of the components of CUT. Analog circuit testing is classified as Simulation before testing and after testing. Simulation before testing approach is based on developing fault dictionary for the possible fault conditions. In [1], fault dictionary based hard fault detection is proposed. The fault dictionary is built by measuring the diagnosis variables for different hard fault conditions and the fault detection is performed on circuits with multiple solutions. In [2], circle equation-based modeling method suitable for locating parametric and hard faults is being proposed. The equation is independent from the value of element to be modeled, and uniquely determined by its location and the nominal values of the remaining elements in the circuit under test. Hence, the circle equation can model any continuous parameter shifting or hard fault occurs. Three points are sufficient to determine a circle; therefore, only three simulations corresponding to three distinct faulty parameters are used to model all parameter shifting faults. In [3], hard faults detection is performed based multi frequency measurements of diagnosis variables. In [4], a wavelet based method is proposed to locate parametric and hard faults in analog circuits. In wavelet analysis of diagnosis variables, two test metrics, one based on a discrimination factor using normalized Euclidean distances and the other utilizing Mahalanobis distances, are introduced and they rely on wavelet energy computation. Tolerance limit, the factor that affects fault detectability, for CUT is set by statistical processing data obtained from a set of fault-free circuits. A test vector based parametric faults detection is performed in [5]. This paper uses the test vector as proposed in [5] but to solve tolerance issue of real time analog circuit testing, test vectors are generated for upper and lower bound values of components of CUT and aim is to locate hard faults. This paper is organized as follows. Section 2 discusses the mathematical background and section 3 explains the test procedure. Section 4 illustrates the proposed method with simulation results obtained on bench mark circuits. Section 5 concludes.

2. MATHEMATICAL FUNDAMENTALS

Fault dictionary based analog circuit testing begins by simulation of CUT and measurement of diagnosis variables for fault free and faulty conditions of components of CUT. Simulation of an electronic circuit involves formulation of circuit equations and solving it for unknowns. To simulate the CUT, Modified Nodal Analysis (MNA) is used. MNA uses the voltage, current relationship of the circuit components and KCL [7, 8]. MNA for linear systems results in the system equation of the form

$$AX = Z \tag{1}$$

where A is the coefficient matrix, X is the unknown vector consists of circuit variables (node voltages and few branch currents) and Z is the excitation matrix. The circuit coefficient matrix is formed by the sub matrices,

$$A = \begin{bmatrix} G & B \\ C & D \end{bmatrix} \tag{2}$$

G is the conductance of the components in the CUT and the values of G are determined by the interconnections of the circuit components. B and C matrices consist of 0, 1,-1 and the values are based on the interconnections of the voltage sources. The D matrix is developed with zeros for independent sources and has nonzero values for dependent sources. The X matrix with variables useful for the diagnosis is formed by the node voltages and the unknown currents through the sources.

$$X = \begin{bmatrix} V_n \\ I_v \end{bmatrix} \tag{3}$$

The right hand side matrix (Z) consists of the values of independent current and voltage sources.

$$Z = \begin{bmatrix} I \\ V \end{bmatrix} \tag{4}$$

The unknown vector is found by solving the linear system equations. In case of circuits with nonlinear devices, the nonlinear devices are modeled using their large signal or DC models [13]. The current through the devices is introduced as a new circuit variable in the unknown vector. The circuit equations obtained from MNA are solved using Newton Raphson (NR) method. To reduce the iteration dependent blocks [9] the nonlinear device equations are arranged as from (5) to (9) and the circuit matrix is formed as in (10). The nonlinear devices are described by their V-I relationship as

$$V = f(I) \tag{5}$$

The Taylor series approximation (neglecting higher order terms) of (5) is,

$$V^{K+1} = V^{K} + (df(I)/dI)^{K} (I^{K+1} - I^{K}) \tag{6}$$

Where K- NR iteration number,

Rearranging (6),

$$V^{K+1} - (df(I)/dI)^{K} I^{K+1} = V^{K} - (df(I)/dI)^{K} I^{K} \tag{7}$$

Let $V^{K} - (df(I)/dI) I^{K} = a^{K}$ (8)

Now (7) becomes

$$V^{K+1} - (df(I)/dI)^{K} I^{K+1} = a^{K} \tag{9}$$

$$\begin{bmatrix} G_{11} & \cdots & G_{1n} & B_{11} \\ \vdots & \cdots & \vdots & \vdots \\ G_{n1} & \cdots & G_{nn} & B_{n1} \\ C_{11} & \cdots & C_{1n} & -(df(I)/dI)^{K} \end{bmatrix} \begin{bmatrix} V_1^{K+1} \\ \vdots \\ I^{K+1} \end{bmatrix} = \begin{bmatrix} \cdot \\ \cdot \\ \cdot \\ a^{K} \end{bmatrix} \tag{10}$$

Faults in the CUT are simulated using Fault Rubber Stamp (FRS) [6, 8, 9]. FRS is based on the MNA stamp of the components of a CUT. The MNA stamp of a component C_n connected in between the nodes j and j' (V_j , V_j'- respective node voltages) ,in the coefficient matrix is,

$$\begin{array}{c} \\ j \\ j' \end{array} \begin{array}{c} \begin{array}{cc} V_j & V_j' \end{array} \\ \begin{bmatrix} +C_n & -C_n \\ -C_n & +C_n \end{bmatrix} \end{array} \tag{11}$$

If this component is assumed to be faulty, its value changes from C_n to $C_n \pm \Delta$. This deviation causes the current through that faulty component to deviate from its nominal value. This current deviation called fault variable (ϕ) is introduced in the faulty circuit unknown matrix as an unknown branch current. To indicate the current deviation through the faulty component, the faulty component is represented as a parallel combination of its nominal value and the deviation (Δ) (fig.1). V_j and V_j' are the node voltages at the nodes j and j' respectively. i_f is the current deviation through the faulty component.

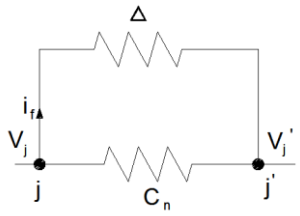

Fig1. *Faulty component representation*

The fault rubber stamp [6, 8, 9] for the component C_n is,

$$\begin{array}{c} \\ j \\ j' \\ \\ f \end{array} \begin{array}{c} \begin{array}{ccc} V_j & V_j' & \end{array} \\ \left[\begin{array}{ccc|c} +C_n & -C_n & \vdots & 1 \\ -C_n & +C_n & \vdots & -1 \\ \cdots & \cdots & \cdots & \cdots \\ \hline 1 & -1 & \vdots & -\Delta^{-1} \end{array}\right] \end{array} \tag{12}$$

The bottom row line is the faulty component equation and the right most column corresponds to the extra fault variable. As seen in (12), for each faulty component there is an additional column at the right side and row at the bottom of the coefficient matrix is introduced. The faulty system with the FRS in matrix form is,

$$\begin{bmatrix} A & c \\ r & \Delta \end{bmatrix} \begin{bmatrix} X_f \\ \phi \end{bmatrix} = \begin{bmatrix} Z \\ 0 \end{bmatrix} \tag{13}$$

where c and r are the additional column and row introduced corresponding to a faulty component. The additional column c indicates the location of the faulty component. The additional row r is the faulty component equation with its node voltages. The value of Δ depends on the faulty value of the component. It can be observed that a new variable called fault variable (ϕ) is also introduced as unknown into the unknown vector matrix (X_f) of the faulty circuit. It can also be noted that this fault variable is the unknown branch current. As seen in (13), the coefficient matrix (A) of the nominal circuit is retained in forming the faulty system equation without any modification in the values of it. Thus from (13), the faulty circuit equations are written as,

$$AX_f + c\phi = Z \tag{14}$$

$$rX_f + \Delta\phi = 0 \tag{15}$$

replacing $Z = AX$ from (1),

$$AX_f + c\phi = AX \tag{16}$$

$$A(X - X_f) = c\phi \tag{17}$$

$$X - X_f = A^{-1}c\phi \tag{18}$$

$$X - X_f = t\phi \tag{19}$$

$$\phi = (X - X_f)/t \tag{20}$$

$$t = A^{-1}c \tag{21}$$

The product $A^{-1}c$ is a column vector and it is called test vector [6]. As c describes the location of a component in the CUT, the test vector is associated to that component and the values are independent of the faults and also the rows are associated to the diagnosis variables or the circuit variables. Thus the fault variable which can be obtained by the element wise division of the difference vector (difference between the nominal and the faulty solutions) and the test vector is also associated to a specific component in the CUT and the diagnosis variables.

3. TEST FLOW

The proposed test procedure consists of two phases. In the first stage the circuit simulation is done to derive the diagnosis variables (X). In real time the components are always with their nominal values

and may be within the tolerance limits. From equation (21), it can be observed that the test vectors are sensitive to component values (circuit matrix A). This limits the fault detectablity if testing is performed with nominal values of components. To solve this, test vectors are generated for upper and lower bound values of components of CUT and these test vectors are treated as fault dictionary. In the second stage called pretesting stage different faulty conditions such as open and short of passive components are introduced into the circuit and diagnosis variables are measured. The diagnosis variables for testing are selected based on the values test vectors. The diagnosis variables with same value test vectors are not useful for testing as they lead to same fault variable. The fault variables corresponding to the components of CUT and the diagnosis variables are estimated using (20) for upper bound and lower bound test vectors. The average and relative standard deviation related to the average value are estimated and found to be the lowest value for faulty components. Figures 2 & 3 show the detailed test flow.

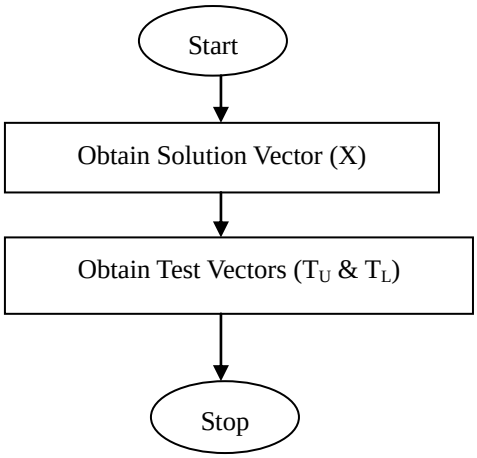

Fig2. *Pre testing stage*

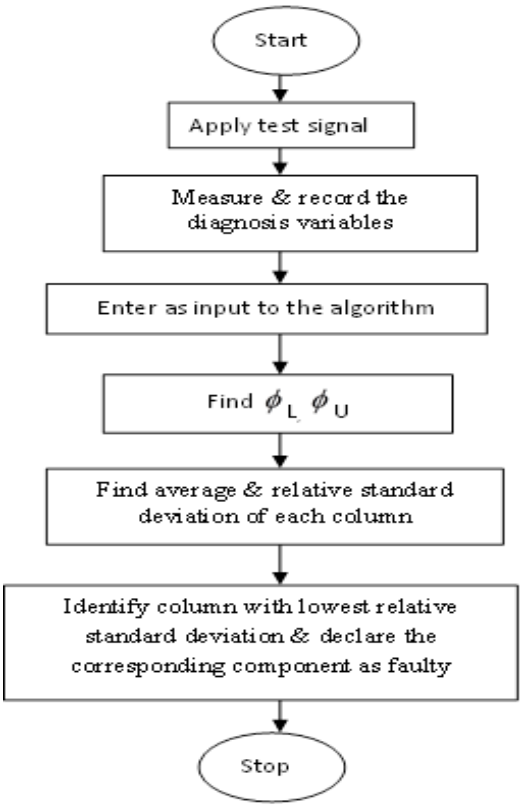

Fig3. *Testing Stage*

4. ILLUSTRATION

The CUT with its nominal value is shown in fig. 4. The diode is modeled using exponential model [5]. A current of 1A is applied at node 1.The circuit equations are assembled using MNA as from (1) to (13). A column vector (c) corresponding to the location of each component is derived and the test vector (only the magnitude) as in (19) is calculated for all the components with upper and lower bound values (fig.5-in logarithmic scale). All the components are assumed to be with 5 % tolerance. Single hard fault conditions are introduced into the CUT and the faulty circuit is simulated. The fault variables corresponding to all the components of Cut are estimated using (20). Fault diagnosis is performed as explained in the flow diagrams 2& 3. Testing is done with the diagnosis variables (node voltages) measured at test nodes 2 & 5. These test nodes are selected by assuming that these are accessible for testing as well as from the values of test vectors. Short circuit hard faults are implemented using 1Ω and open circuit hard faults are implemented using 200MΩ. The average and relative standard deviation of each fault variable are obtained and are listed in table 1. From the table it can be observed that the relative standard deviation is the lowest value for the specific fault type. For example, the faulty condition R_1 short circuit leads to the relative standard deviation of the fault variables corresponding to the components of CUT as 2.3E-15, 1.2,1.15, 1.2,1.2,1.2,1.2 (R_1, R_2, R_3 , R_4, R_5, R_6, R_7) and it can be followed that the lowest value is found for R_1. Hence R_1 is faulty.

Table1. *Results of Diode Circuit*

Fault Type	Relative Standard Deviation of Fault Variables corresponding to components of CUT						
	R_1	**R_2**	**R_3**	**R_4**	**R_5**	**R_6**	**R_7**
R_1 Short	2.3E-5	1.2	1.15	1.2	1.2	1.2	1.2
R_2 Short	1.15	0.057	0.27	0.8	1.1	1.12	0.98
R_3 Short	1.2	0.27	0.055	0.54	1.06	1.1	0.88
R_4 Short	1.15	0.64	0.63	0.058	0.89	1.33	0.45
R_2 Open	1.16	0.058	0.27	0.8	1.1	1.12	0.98
R_5 Open	1.55	1.1	1.06	0.89	0.057	0.38	0.62
R_6 Open	1.2	1.12	1.1	0.97	0.27	0.058	0.8
R_7 Open	1.2	0.98	0.89	0.45	0.63	0.79	0.057
R_1 Open	0.058	1.157	1.16	1.158	1.159	1.2	1.21
R_4 Open	1.15	0.79	0.63	0.058	0.89	0.97	0.44
R_5 short	1.16	1.10	1.06	0.88	0.058	0.27	0.47
R_6 Short	1.15	1.12	1.1	0.97	0.28	0.0577	0.79
R_7 Short	1.15	0.98	0.88	0.45	0.63	0.79	0.057
R_3 Open	1.15	0.29	0.048	0.6	1.06	1.09	0.87

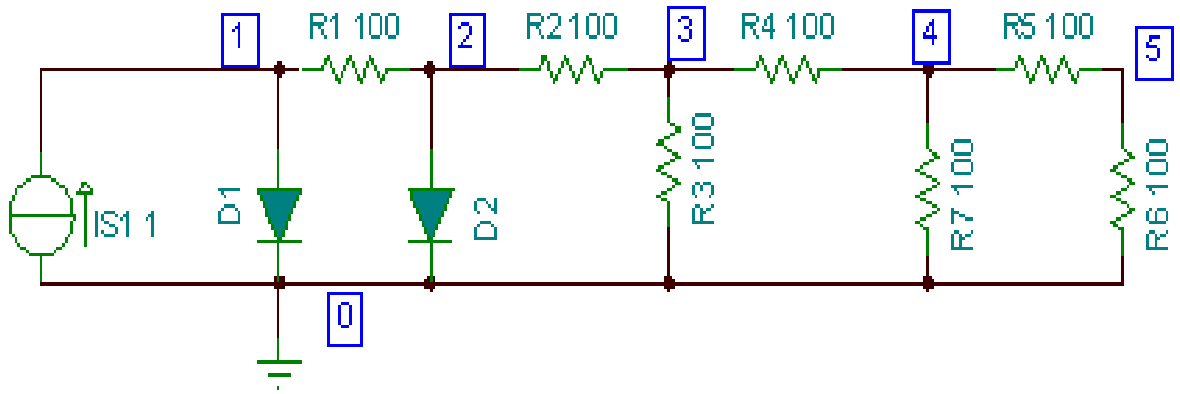

Fig4. *Diode Circuit*

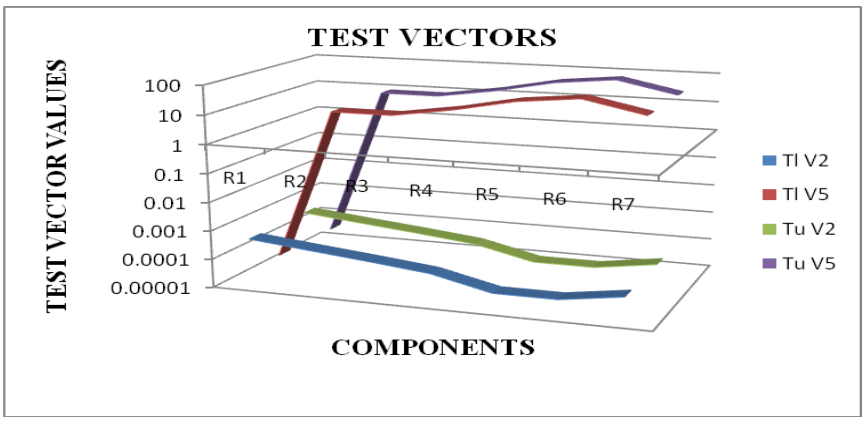

Fig5. *Test Vectors*

5. CONCLUSION

A method to locate single hard fault based on fault dictionary in non linear analog circuits is proposed. Fault dictionary is built by deriving the test vectors associated with the components of CUT where as in case of conventional fault dictionary; the diagnosis variables are measured and stored for different faulty conditions of components of CUT which require larger data base and higher computational cost. But the proposed approach requires only the test vectors corresponding to the diagnosis variables for testing. This reduces the requirement of larger data base and high computational cost. The hard faults conditions of passive components of CUT are identified with the test vectors with the simple test procedure. And it can also be observed that the approach do not require any special procedures to determine or select the diagnosis variables for testing and they can be determined from the test variables.

REFERENCES

[1] Michał Tadeusiewicz · Andrzej Kuczy´ nski, Stanisław Hałgas, “Catastrophic Fault Diagnosis of a Certain Class of Nonlinear Analog Circuits”, Circuits, Syst. Signal Processing, 2015, 34, 353-375.

[2] Shulin Tian, ChengLin Yang, Fanq Chen, Zhen Liu, “Circle Equation Based Fault Modeling Method for Linear Analog Circuits”, IEEE Transactions on Instrumentation and Measurement, 63 (9):2145-2159, 2014.

[3] M. Peng, C.K. Tse, M. Shen, K. Xie, “Fault diagnosis of analog circuits using systematic tests based on data fusion”, Circuits Syst. Signal Process, 2013, 32, 525–539.

[4] A.D. Spyronasios, M.G. Dimopoulos, A.A. Hatzopoulos, “Wavelet analysis for the detection of parametric and catastrophic faults in mixed-signal circuits”, IEEE Trans. Instrum. Meas., 2011, 60, 2025–2038.

[5] Adel S. Sedra, Kenneth Carless Smith, Microelectronic Circuits, Oxford University Press, 2004.

[6] Jose A.Soares Augusto and Carlos Beltran Almeida, “A Tool for Single-Fault Diagnosis in Linear Analog Circuits with Tolerance Using the T-vector Approach”, Hindawi Publishing Corporation, VLSI design, 2008, pp 1-8.

[7] C.-W.Ho, A.Ruehli and P.Brennan, “The modified nodal approach to network analysis”, IEEE Transactions on Circuits and Systems, 1975, Vol.22, no.6, pp.504-509.

[8] Jiri Vilach and Kishore Singhal, Computer methods for circuit analysis and design, Van Nostrand Reinhold Company, 1983.

[9] J. S. Augusto, C. B. Almeida, "FASTNR: An Efficient Fault Simulator for Linear and Nonlinear Circuits" VLSI'99 ("VLSI: Systems on a Chip", Kluwer), Lisboa, Portugal, 1999.

AUTHORS' BIOGRAPHY

Ms.G.Puvaneswari is currently working as an Assistant Professor (Senior Grade) at Coimbatore Institute of Technology, Coimbatore, India. She holds more than 15 years of teaching experience. Her research interests are Analog circuits design and testing, Biomedical Engineering. She did her Bachelor's degree in Electronics and Communication Engineering at R.M.K.Enginnering College, Madras University in April 1999 and Master's degree in Medical Electronics at College of Engineering, Guindy, Anna University, Chennai in July 2005.

Dr.S.Uma Maheswari is presently working as an Associate Professor in the Department of Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore, India. She holds more than 25 years of teaching experience. Her research interests are VLSI Design, Digital Image Processing and Digital Signal Processing. She obtained her doctoral degree in Electrical and Electronics Engineering with specialization in Biometrics, from Bharathiar University. Coimbatore. She obtained her Masters Degree in Applied Electronics from Coimbatore Institute of Technology, March 1991 and Bachelor's Degree in Electronics and Communication Engineering from Government College of Technology in 1985.