International Journal of Research Studies in Science, Engineering and Technology
Volume 2, Issue 6, June 2015, PP 110-112
ISSN 2349-4751 (Print) & ISSN 2349-476X (Online)

Design of High Speed Hybridized Multiplier

Prof.P.A.Jadhav

Department of Electronics Engg., YCCE, Nagpur
ja_pradnya@yahoo.com

ProfV.B. Niranjane

Department of ET., Y.C.C.E Nagpur
niranjane_vaishali@yahoo.com

Prof.Kalyani Ingole

Department of ET,
K.D.K College of Engg, Nagpur

Abstract: *The key problem VLSI circuits are high power consumption, larger area utilization and delay which affect the speed of computation and also result in power dissipation.. In general, speed and power are the essential factor in VLSI design. For solving the issues, a new architecture has been proposed in which the proposed system, high speed multiplier, modified booth multiplier and Wallace tree multiplier are hybridized with carry look ahead adder and formed a hybridized multiplier which delivers high speed computation with low power consumption. Modified booth multiplier is proposed to reduce the partial product where as a Wallace tree multiplier is accompanied for fast addition and CLA used for final accumulation..The actual hybridized multiplier is a combination of Wallace tree and booth multiplier.*

Keywords: *Modified Booth Multiplier; Wallace tree multiplier, Carry Look-ahead Adder, Hybrid Architecture.*

1. INTRODUCTION

The essential need of VLSI circuits is high speed computation and low power consumption. Achieving the optimized result is highly challengeable since it is difficult to select and optimize Multipliers and adders which are responsible for computation. Multipliers and adders play an important role in VLSI for getting desired results. Multiplication is a series repeated additions. Multiplicand is the number to be added, Multiplier is the number of times that it is to be added and product is the result. Partial product is generated at every step. The output of multiplicand X and the multiplier Y is the partial product of both X and Y. At first the partial products will be generated till all the operands and get added. After the generation the partial products are added then the final accumulation will takes place.

A new architecture has been proposed by the hybridization of modified booth encoder, Wallace tree multiplier and carry Look-ahead adder. This hybrid multiplier is mainly focused for reducing the partial products and to trigger the speed of the computation. MBM generates n/2 partial products for 'n' inputs so the area is directly reduced and increases the speed of the computation. Wallace tree is designed to carry save adders (CSA) which is used for fast addition since 3:2 compressors are used. It is responsible for fast addition. The results of CSA are finally getting computed by Carry Look-ahead adder which is mainly proposed for final accumulation.

2. LITERATURE SURVEY

After analyzing the literature survey it is clearly found that there is no sophisticated system for low power and high speed computation. Selection of multipliers is important for achieving optimized results. Bypass technique is combined with Wallace tree multiplier for overcoming the shortcomings but the result is not up to the mark since no steps involved in reduction of partial products. Power reduction technique is used in order to suppress the power consumption. It results in suppression of power but no improvement in computation speed. Parallel processing is focused by using pipelined multipliers which are expected to deliver high speed and low power. Since the operation is pipelined the area of the design is increased. It is well known that area is inversely proportional to the speed so it affects the speed.

The comparative study of the multipliers is done. The results point out the superior multiplier in terms of speed, area and delay. A new architecture has been designed by using the combination of Wallace

tree multiplier and modified booth multiplier for low power and high speed. It delivers moderate speed with power reduction but there is no reduction in Partial products. Array multiplier is also proposed for meeting the challenges by modifying its structure. It results in maximum area utilization so the speed cannot the improved. SPST multiplier is used for overcoming the drawbacks and produces good results when comparing with array multiplier and modified booth multiplier.

3. HYBRID ARCHITECTURE

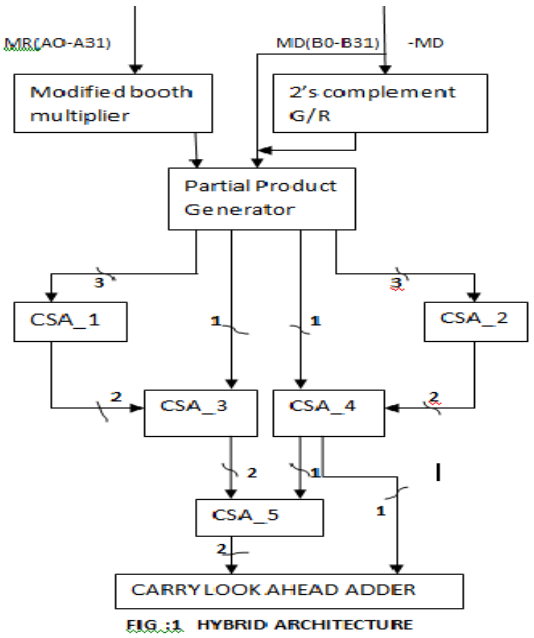

FIG :1 HYBRID ARCHITECTURE

3.1. Modified Booth Multiplier

The modified booth multiplier has a powerful algorithm for signed-number multiplication, which treats both positive and negative number uniformly. Actually a combination of the three different bits is arranged and with respective to that a standard bit pattern is allowed.

MULTIPLIERS BIT	RECODED BIT
000	0XA
001	1XA
010	1XA
011	2XA
100	-2XA
101	-1XA
110	-1XA
111	0XA

3.2. 2's Complement Generator

When the input is signed ,The 2,s complement of that number will be taken then it will be processed for generating outputs i.e exactly solving simple traditional method by using 1,s complement and adding 1 in generated output.

3.3. Partial Product Generator

Partial product reduction takes place in a booth algorithm by the efficient encoding method. This algorithm can save multiplier layout area reduced delay at the same time.

3.4. Carry Save Adder

It is a type of digital adder use in computer micro architecture to compute the some of three or more n bit number in binary.

3.5. Carry Look Ahead Adder

It is used in digital logic .It improves speed by reducing time required to determine the carry bits.

4. WALLACE TREE MULTIPLIER

It is an efficient hardware implement of digital circuit that multiplies two integer .It reduced the number of partial product to two layers of an full adder and half adder .The Wallace tree multiplier has irregular interconnections that's why they can consumes or occupies more area on the wafer and needs greater space for cell interconnections wirings. It is used for designing of CSA which is used for fast addition .The exact output of Wallace tree multipliers are in the form of one or two forms of wires. Just as 3:2 decoders.

5. IMPLEMENTATION

The codes for hybridized multiplier written in VHDL language and implemented on XILIX 13.4.Experimental result shows delay for proposed structure 37.067 ns and conventional multiplier delay is 47.05 ns on Spartan 6.

6. CONCLUSION

The Hybrid Architecture is the combination of high speed multipliers and adders. The design can be used for meeting the challenges in all signal processing applications by its faster operations. The speed of the computation is increased since the partial products are reduced.

REFERENCES

[1] Madhav Thiyagarajan , "Low power high speed multiplier using parallel multiplication", *International Journal of VLSI Design*, Vol:2, Issue:1, pp:75-78, 2011.

[2] Praveen Kumar.M and Ashok Babu.K, "A spurious-power suppression technique for multimedia/dsp applications", *International journal of advanced engineering sciences and technologies.*

[3] 3.Shyh-Jye Jou, Chang-Yu Chen, En-Chung Yang and Chau-Chin Su , "A pipelined multiplier-accumulator using a high-speed, low-power static and dynamic full adder design'', *IEEE Journal of Solid-State Circuits,* Vol:32, Issue:1, pp:114– 118, 1997.

[4] SumitVaidya1 and Deepak Dandekar, ''Delay-power performance comparison of multipliers in vlsi circuit design'', *International journal of computer networks and communication,* Vol: 2, Issue: 4, pp: 47-56, 2010.

[5] Vinoth.C, '' a novel low power and high speed Wallace tree multiplier for RISC processor'', *IEEE trans on Electronics Computer Technology*, Vol: 1, pp: 230-234**,** 2011.

[6] Wang J.S, Kuo C.N and Yang T.H, "Low-power fixed-width array multipliers", *International Symposium. On Low Power Electron is Design*, pp: 307–312, 2004.