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Digital Soft-Start PSM Buck Converter

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Abstract: *Although a typical PWM controller is well known for its good regulation capabilities, inrush current and overshoot voltage during start-up period as well as high switching losses at low loads are some of the major factors affecting its otherwise good performance. Therefore in this paper a simple Soft-start pulse skipping modulation (SSPSM) scheme implemented on a typical buck converter is presented to deal with the above mentioned problems. A soft-start scheme was designed to prevent the instantaneous rise of Vref from zero to full value and this was combined with a Pulse Skipping Modulation (PSM) logic circuit to reduce the switching losses at low loads. The proposed SSPSM buck converter was modeled and simulated in Matlab Simulink and the results clearly shows that the circuit was able to elongate the rise of Vref from zero to its maximum value thereby effectively eliminating inrush current and overshoot voltage. During steady state at low loads the circuit was shown to be able to skip some pulses thereby keeping the converter switch off for longer periods hence reducing the frequency of opening and closing of the switch.*

Keywords: *Soft-start scheme, Pulse Skipping Modulation (PSM), Soft-start Pulse Skipping Modulation (SSPSM), Inrush current, Overshoot voltage, DC-DC converter.*

1. INTRODUCTION

The phenomenal advancement in technology has given rise to modern electronic systems that require reliable, high quality, efficient, small and lightweight power supply systems. This has inspired the widespread use of DC-DC converters in many industrial and electrical systems. The Buck converter is one type of DC-DC converter which has found wide usage in digital systems due to its high efficiency which makes it suitable for use in areas where losses cannot be tolerated. A voltage mode PWM controller is usually used to control the output voltage of the Buck converter by altering the duty cycle of the control switch in accordance with the error between the measured output voltage and the desired output voltage commonly known as reference voltage Vref [1]. Even though the conventional PWM controlled converter is widely used due to its good regulation characteristics there are two major problems associated with it. (1) At startup up there is the problem of inrush current and overshoot voltages [2-5] (2) during steady state operation there is the problem of switching losses due to the high speed of opening and closing of the switch especially when operating at low loads [8].

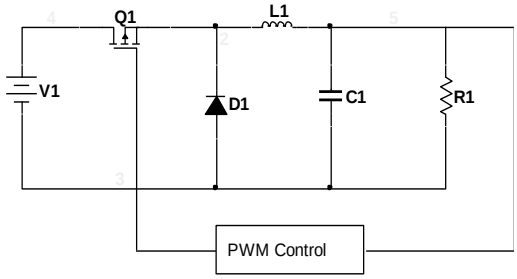

Figure1. *Typical PWM controlled Buck converter*

2. INRUSH CURRENT AND OVERSHOOT VOLTAGE PROBLEM

A typical DC-DC converter such as the one shown in Figure 1 consists of at least one transistor switch and a PWM controller to control the switch, a diode switch, an inductor and capacitor

combination output filter. The converter works by translating the error signal into a variable duty cycle in order to maintain a constant voltage at the output. However, the conventional circuit has one inherent drawback during the "start-up" period. At the beginning of the start-up transient the output voltage is zero and V_{out} needs to rise from its initial zero value until it reaches its designated output value. Because the output voltage is much lower than the desired output voltage the error amplifier is unbalanced and the duty cycle of the switch is very high. A 100% duty cycle can cause the inductor current to rise high above its equilibrium value and this is what is known as inrush current. Once the inrush current is present, it remains for a short while because the inductor cannot change instantaneously. The presence of this inrush current may cause the output voltage to momentarily rise above its regulated value and this is what is known as overshoot voltage. This momentary excessive current and voltage can cause damage to the regulator circuit during start up and is undesirable. In order to mitigate against the damages that can be caused by the inrush current and overshoot voltage the principle of soft-start is usually applied in the dc-dc converters. The principle of the soft-start scheme entails that the duty cycle of the switch regulator rises from the initial zero value to normal operation value in a controlled manner. This will help to prevent the emergency of inrush current and overshoot voltage thereby protecting the inductor, capacitor and switches from suffering damages during the regulator start-up operation. Many soft-start schemes have been proposed [2-7] and the disadvantages of the conventional soft-start method have been widely elucidated [11]. And in this paper a simple pulse controlled method of soft-start which overcomes the shortfalls of the conventional soft-start methods is proposed for a typical buck converter system [9].

3. Problem of Switching Losses

The major goal of a DC-DC converter during steady operation is to regulate the output voltage in spite of changes in the load and/or input voltage. This is typically achieved by adjusting the duty cycle of the PWM signal to counteract any changes between the designated output voltage and the measured output voltage. In voltage regulation efficiency is one of the most important characteristics of a regulator. Also minimizing losses in a voltage regulation process is of paramount importance in converter design. The main sources of power losses in a typical switching converter consist of [12]: (1) load dependent losses /conduction losses- these are typically losses due to MOSFET on resistance and inductor winding resistance. (2) load independent losses – these can be divided into (a) switching loss which are typically losses due to MOSFET output capacitance, MOSFET gate capacitance, inductor core loss, and gate driver loss and (b) fixed losses- which are typically losses due to MOSFET leakage current.

Generally a typical DC-DC converter shown in Fig1 is very efficient under heavy and medium loads however it is not very efficient when operating with lighter loads. As can be seen from the above list one of the major contributors of that inefficiency is the inherent capacitance and resistance of the switch. The purpose of the controller is to adjust the duty cycle of the PWM signal to regulate the output voltage in accordance with the error signal. If the feedback signal indicates a decrease in the level of the load output, the controller's modulating responds is to reduce the width of the modulating pulses and this causes a reduction in the power delivered to the load. However, there is a limit as to how much the width of a single pulse of the PWM signal can be decreased. In a fixed-frequency converter at light load conditions, switching loss is the most dominant source of power loss during steady state. Where the load level has decreased to a point where it is impossible to reduce the pulse width further, 'burst-mode' operation has been used to achieve voltage regulation [13]. However in this paper a simple technique for pulse-skipping is proposed for a typical switching power converter.

3.1. Principles of Pulse Skipping

Pulse Skipping Modulation (PSM) is one of the techniques applied to reduce switching losses and improve the efficiency of a typical switch converter. By keeping the MOSFETs in the off-state for several switch cycles the switching losses in the MOSFET switch and gate driver circuit are reduced while maintaining a good voltage regulation at the output for a DC-DC converter operating under light loads or under standby conditions.

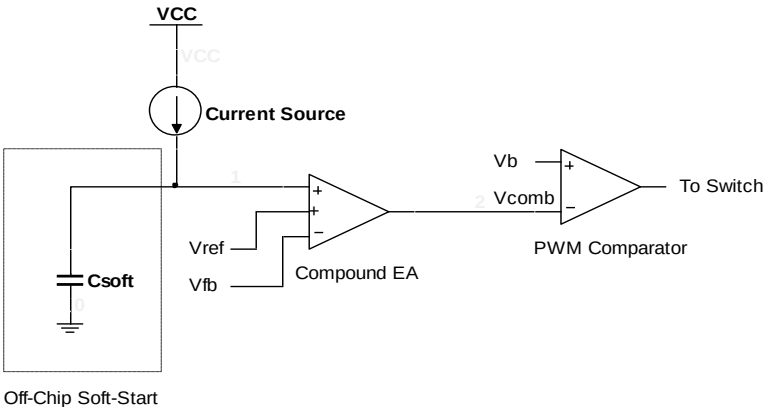

Figure2. *Diagram of the conventional soft start method*

4. PROPOSED PULSE CONTROLLED SOFT-START METHOD

In order to rectify the problem of inrush current and overshoot voltage the conventional soft-start scheme, Figure 2, works to prevent excess current from flowing through the components by gradually varying the reference voltage(Ramped reference voltage) at start up. The ramped reference voltage is produced by charging a capacitor with a constant current of small value, unfortunately capacitor voltage from which the ramped reference is obtained is too big to be on the system's chip, hence it has to be provided for as an off chip component. The additional off chip capacitor has the effect of increasing the size as well as the cost of the buck converter which is clearly a disadvantage in portable applications.

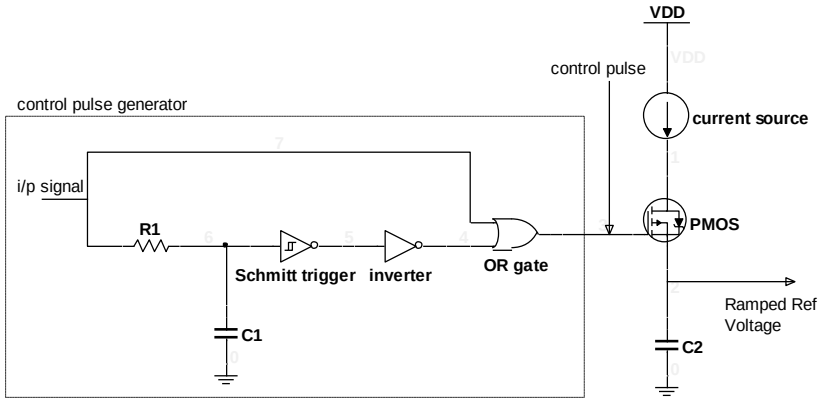

Figure3. *Pulse Controlled Soft-start scheme*

Therefore in this paper a pulse controlled soft start(PCSS) scheme with no off-chip components which generates a ramped reference voltage to provide a soft start for a typical buck converter is proposed. The proposed PCSS scheme shown in Figure 3 consists of a current source that is connected to a positive voltage supply, a capacitor connected to the ground and a switch that serially connects the current source and the capacitor. A control pulse generator(CPG) produces a control pulse that regulates the switch ensuring that a pulsed current is supplied to the capacitor from the current source.

The CPG contains a capacitor and a resistor which introduces a delay in the processing of the signal, a schmitt trigger forwards the signal to the output and an inverter inverts the signal before it is ORed together with the undelayed signal by an OR logic gate. The output of the OR gate gives us the control pulse that controls the switch. The capcitor is charged by the pulsed current and the switch serves to control the charging of the capacitor. The voltage across the capacitor gives us the ramped reference voltage and the slope of the ramped reference voltage is dertemined by the turn on and turn off periods of the Switch.

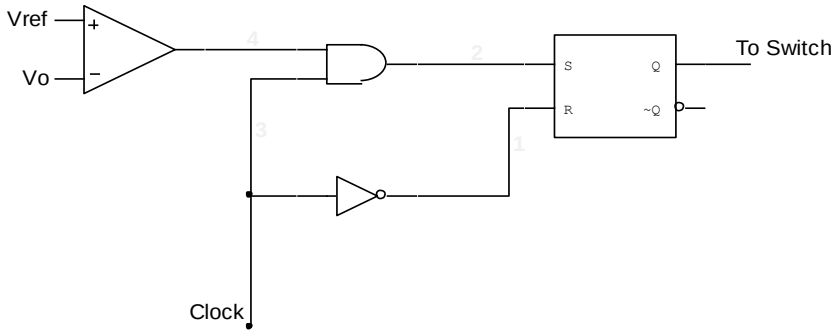

Figure4. *Diagram of PSM control circuit*

5. PSM CIRCUIT OPERATION

The PSM logic circuit is shown in Figure 4 and its basic operation is that when the output voltage is below the reference voltage Vref, then PSM control logic allows the Controller circuit to operate as a normal PWM circuit by permitting the clock pulses to pass through and control the switch. When the output voltage is above Vref the PSM logic makes the Controller operate in PSM mode by blocking the pulses generated by the clock from reaching the switch hence making the switch skip some pulses thereby maintaining an off state on the switch for a longer period. This reduces the current to the inductor and ultimately the output to reduce the high output voltage to Vref. Exactly how does the PSM logic circuit make the controller skip some pulses? The PSM logic circuit consists of a comparator/Error amplifier whose inverting input is connected to the measured output voltage known as feedback and the non-inverting input is connected to the reference voltage which in our case is a ramped reference voltage from the soft-start circuit during start-up and a constant Vref during steady-state. The output from the comparator is fed into an AND logic gate whose other input receives clock pulses of a constant frequency and a constant width from the system clock. [14].The output from the AND gate feeds into an SR flip flop whose other input also receives clock pulses from the system clock. The SR flip flop is coupled to the buck converter switch to control its opening and closing periods.

As can be seen in Figure 4, Vo is compared with vref by a comparator and the output is ANDed with a CLK. When the reference voltage Vref is higher than the output voltage Vo (Vref>Vo) the comparator output is HIGH implying that the AND gate output is HIGH whenever the Clock pulse CLK is HIGH. This also means the SR flip-flop is set whenever the clock is HIGH and is reset whenever the clock pulse is LOW implying that the controller works as a normal PWM circuit during the charging period. When the reference voltage Vref is smaller than the output voltage Vo(Vref<Vo), the output from the comparator is LOW and this means that, it doesn't matter whether the clock pulse is HIGH or LOW the output of the AND gate will remain LOW. Therefore the SR flip flop is not set and no pulses are sent to the switch. The pulses that are not sent to the switch are said to have been skipped hence the term 'Pulse Skipping' and the time when the pulses are blocked from reaching the switch is known as skipping period. By skipping pulses when Vo is greater than Vref, this means the switch is kept on the

'OFF' state for longer periods reducing the current to the inductor thereby reducing the output voltage which quickly brings it down to the designated value. Thus by alternately allowing certain pulses p and skipping other pulses q the voltage at the output is maintained as close as possible to the reference value thereby maintaining a constant voltage at the output.

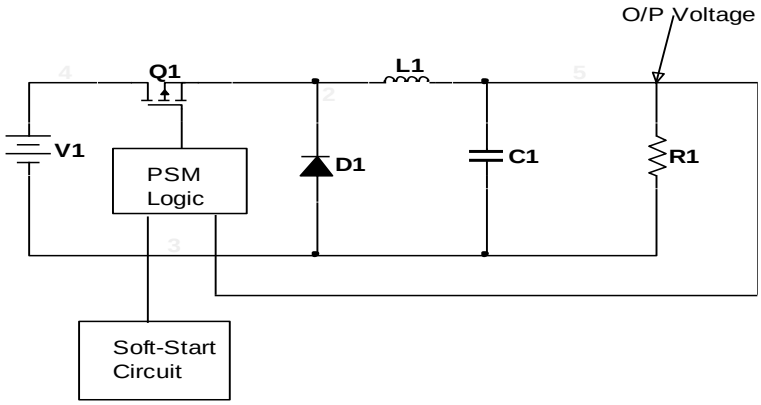

Figure5. *SSPSM buck converter*

6. Mathematical Modeling of The SSPSM Buck Converter

For the soft-start circuit, the slope of the ramped reference voltage, $V_{rampref}$, can be obtained as follows [10]: If the period of the controlling pulse to the switch is T, with duty cycle D, the pulsed current is $I=V_{const}/R_2$, R_2 is the resistance of the current source, C_1 is the CPG capacitor and the output capacitor is C_2, then the capacitor charges by $(IDT)/C_2$. The slope of $V_{rampref}$ is given by

$$slope = {}^{ID}/_{C_2} \tag{1}$$

Substituting the value of $D=KR_1C_1/T$ and $I=V_{const}/R_2$ into the equation (1) gives $V_{const}(KR_1C_1)/(TC_2R_2)$. Therefore the slope of $V_{rampref}$ is given as

$$Slope = {}^{R_1C_1V_{const}K}/_{R_2C_2T} \tag{2}$$

For the PSM logic the model equations were obtained using state space equations and state space averaging method for a converter operating in CCM mode [14]. For *p* cycles the converter operates in the normal "on-off*"* switching state, while for *q* cycles the pulses are skipped keeping the converter in the "off*"* state. Assuming a large working period Tw=(p+q)T, pT is the charging period and qT is the skipping period.

During charging period, pT

$$\dot{x} = A_1x + B_1v_{in} \;\; 0 \le t \le DT, \; y = C_1x \tag{3}$$

$$\dot{x} = A_2 + B_2v_{in} \;\; DT \le t \le T, \; y = C_2x \tag{4}$$

During skipping period, qT

$$\dot{x} = A_2x + B_2v_{in} \;\; 0 \le t \le T, \; y = C_2x \tag{5}$$

Where $A_1 = A_2 = A = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}, x = \begin{bmatrix} i_L \\ V_c \end{bmatrix}, y = v_o$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}, B_2 = 0\ , C = [0 \quad 1]$$

After state space averaging,

$$\dot{x} = Ax + {}^{p}/_{p+q} BDv_{in} \tag{6}$$

If we define the Modulation Factor M, as

$$M = {}^{q}/_{p+q} \tag{7}$$

Then equation 6 becomes

$$\dot{x} = Ax + (1 = M)DBv_{in} \tag{8}$$

Therefore the average output voltage is defined by

$$V_o = (1 - M)Dv_{in} \tag{9}$$

7. Simulation Results

The following parameters were used in the simulation of the Soft-Start PSM converter

L = 4.2 µH, R_L = 80 mΩ, C = 380 µF, R_{esr} = 5 mΩ, f = 150 KHz, V_{in} = 12 V, D = 0.42, Load R = 20 Ω

Figure 6 shows the output of the PSM Logic clearly showing how some pulses are skipped to regulate the output voltage when Vo is higher than Vref. But when Vref is higher than Vo the output from the PSM logic scheme is just a PWM/clock output. Figure 7 shows the output of a PWM controlled buck converter operated in open loop. Figure 8 shows the output of a PSM controlled buck converter operated in open loop. The waveform clearly shows that with PSM the output reaches steady state faster than with PWM although there is an increase in fluctuations in the output voltage and current. Without the soft-start the inrush current and overshoot voltage is seen during the transient stage. Figure 9 shows the output waveform of the buck converter with soft-start with a gentle ramp voltage slope. The waveform clearly shows that the inrush current and overshoot voltage is eliminated but the system takes longer to reach steady state. Figure 10 the output waveform with a steeper Vramp slope and in this case the system reaches steady state much faster whilst at the same time eliminating the overshoot voltage and inrush current however the fluctuations in the output current are a little bit higher. So in designing the best compromise between the desire to have a short transient period and lower harmonics has to be selected. From the results obtained from the simulation it can be clearly seen that the proposed SSPSM buck converter managed to eliminate inrush current and overshoot voltage during the start-up period at the same term reducing the switching losses during steady-state operation by operating in PSM mode when Vref is high than Vo.

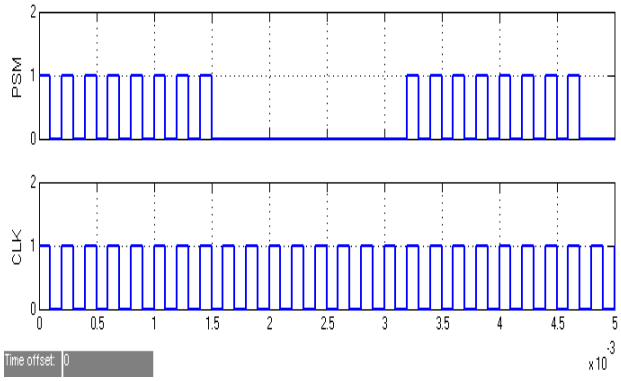

Figure6. *PSM and Clock outputs*

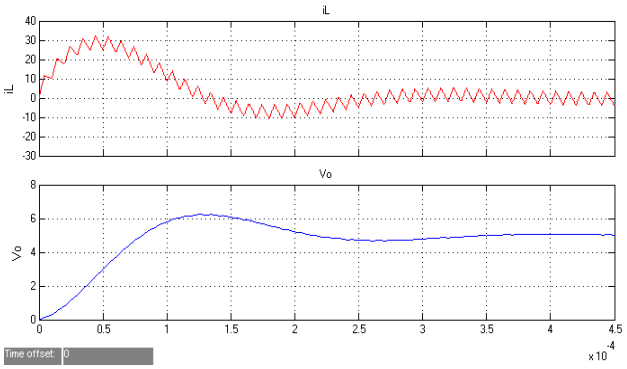

Figure7. *PWM output, open loop*

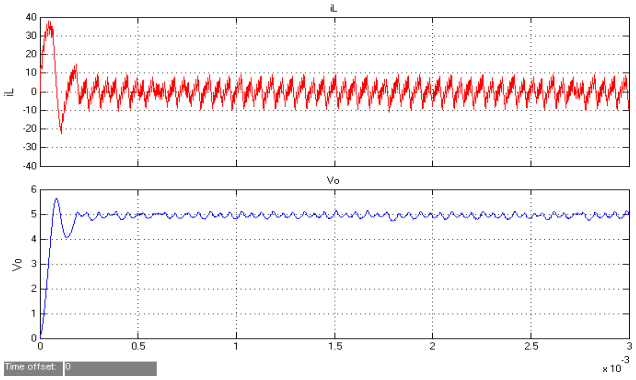

Figure8. *PSM Logic without soft start*

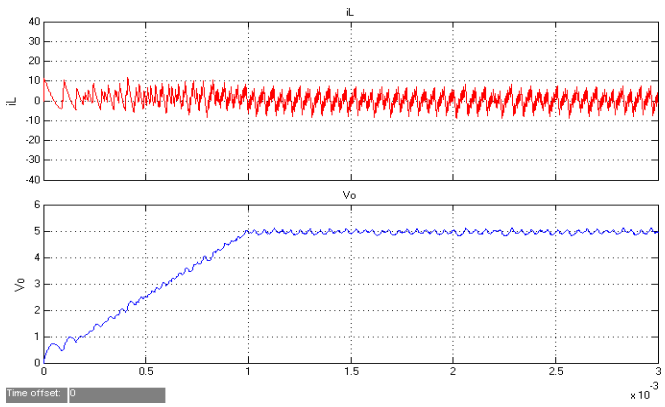

Figure9. *Soft-start output*

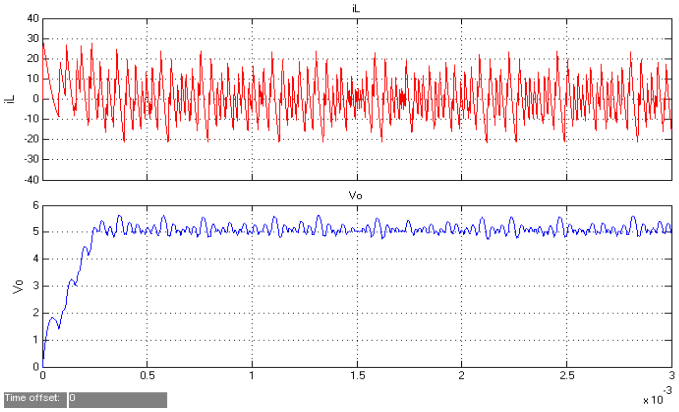

Figure10. *Soft-Start with increased ramp voltage slope (steeper slope)*

8. CONCLUSION

In this paper a simple Soft-start PSM controlled buck converter was proposed, modeled and simulated. The SSPSM converter consisted of a pulse controlled soft-start scheme to deal with the inrush current and overshoot voltage at startup and a PSM logic scheme to deal with switching losses when the buck converter is operating at low loads in steady state. From the results obtained it was proved that the proposed SSPSM system successfully managed to suppress inrush current and overshoot voltage during start-up. It was also shown that the proposed PSM logic managed to skip some pulses when operating at low loads thereby reducing the on-off frequency of the switch which in turn would reduce the switching losses of the converter. Therefore this system was shown to be able to protect the converter from damages caused by inrush current and overshoot voltage at the same time improving the efficiency of the converter especially when operating at low loads.

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