

# Area Foreshorten PDF Estimator with Non-Parametric Technique

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**Abstract:** Adaptive systems are increasing as they employ in different applications which should be able to adopt the real time stipulations. There by the proper statistical building block is necessary. Basically these statistical building blocks are classified by two categories namely parametric and non-parametric. These parametric statistical building blocks even though give smoother statistical curve but they estimated for the stipulated known model there by causes the issues like degrading the adaptive nature and consumes more operation time. There by the non-parametric approach will be the promising solution for the present adaptive natured systems even though this method to a lesser extent accuracy with lesser number of samples. In this paper we introduce the novel architecture for designing alkali histogram unit efficiently. By this the natured feature can be heightened like accelerated speed, expanse and power.

**Keywords:** Probability density function; Adaptive systems; Priority Encoder.

## 1. INTRODUCTION

As the requirements of the end users and processing units are increasing there by causes the advance consideration with reference to that of the calculated evaluations. These are namely called as the adaptive systems. Whenever this adaptive systems are increasing there by the features are also increases. Basically the adaptive refers to acquire the run time decision with refer to the particular environment behavior and characteristic. In order to gain the specified changes referred to that of the reconciling the scenarios. For fulfill these requirements these systems reckons on the estimators. Basically the estimator main functionality is to provide the specified statistics for the behavior of that particular system refers to the adaptive nature of the produced characteristic system

In general these estimators play an important role in different application. Machine learning the term machine learning refers as analyzing the behavior of the system like speed, power, delay input and output characteristic evaluation can be carried out. As the machine controlling when the power factor is increased that many respective capacitive load can be turned ON.

In other application like image processing, tumors are difficult medicate because in older days open surgeries were performed but now key hole surgeries are preferred. The major problem that associated with keyhole medication perfect dimensions of tumor should be necessary. For that aspect also the estimators are required.

Not only above stated application have they plenty liked DSP, computer security, communications, network routings, protocol, digital methods etc.

There by the important estimator are required demandingly for those different designs were proposed previous. But they are not that much suited for the adaptive nature and also on foot back concern to the traditional calculations. Hence we propose the advance method that can be able fulfill for the different applications.

This paper organized as chapter-I deal about the introduction, chapter-II describes the estimator methodology, chapter-III the proposed method followed by the results and discussion, conclusion and references.

## 2. ESTIMATOR METHODOLOGY

Estimators are nothing but the function that acquires the group of exchangeable events that occurred in particular unit area. These estimators are basically two types parametric and non-parametric. In Parametric estimators statistics can be done with the specific demanded known model, by this which give the good response even though for the fewer samples. But as discussed above they try to equip in the known framework there by the drawback concern with the adaptive nature. In order to design a statistical unit for the high end adaptive nature this systems can't be suggested.

In such situation one and only promising approach is nothing but the non-parametric estimation. In this tries itself included with the statistical calculations.

Moreover the operation of the statistical calculation can be carried out by the serial and parallel approaches. In serial approaches the data can be considered in serial manner and in parallel the data can be processed in parallel form. The serial method as it works bit by bit operation that consumes the more statistical time. Hence we prefer the parallel method for advanced adaptive systems.

This non-parametric approach also can be done in two ways cumulative and non-cumulative.

In non- cumulative distribution the statistical calculation can be done for the each window and the previous calculations can be erased before considering the new samples.

The cumulative distribution even though new window samples arrived for the statistical calculation which does not erased previous repeated events, those also can considered for the calculation of the histogram.

In order to find the statistics we need to hold the data for some time for the processing and characterization. Whenever if we heard about the storing data generally we prefer register, but in this case each time we need to remove the old data and new data should be stored. Each time generating the addresses for the reading and writing is critical and some functional block should be necessary. In order to make easy consideration for the storing we prefer FIFO as the hard block element.

Even though the FIFO is well suited for our requirements, but bare FIFO cannot be used in this enabled write can be adopted for desired functionality.

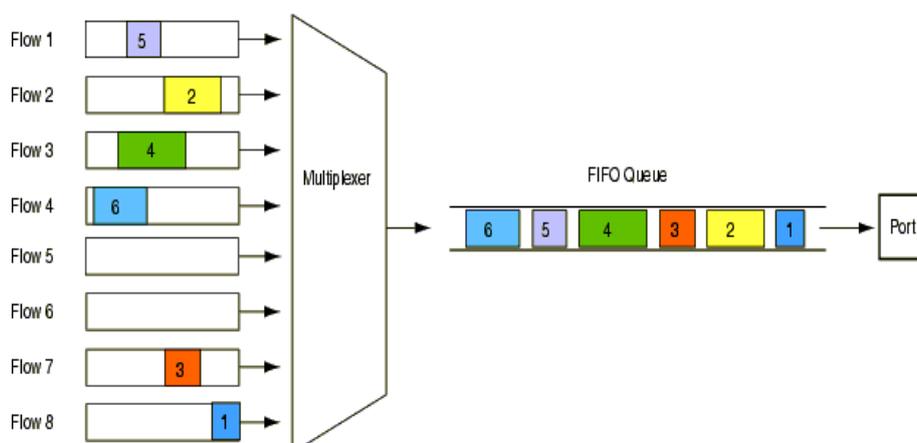


Figure1. Proposed FIFO

## 3. PROPOSED METHOD

As from the previous method we observed that those will introduces latency concern with new sample arrive and comparison with the stored data in all locations.

Figure 2 deals with the histogram calculation circuit when the new sample arrived then it give as the input to the all comparators connected at the individual locations of the FIFO, when comparator takes two inputs new sample and stored sample and provide the output equal or not. Like all the comparators outputs are connected to the AND gate when all input are not equal then that sample to be stored that will gives as enable input to the FIFO control unit. Then the FIFO control unit generates corresponding WR enable and write pointer (address) then that particular sample stored in the corresponding location. If similar sample occurred and gate output goes low then that sample will not stored in the FIFO and corresponding access pattr will be generated for the increase of the respective (bin) counter.

For the access patterns will be generated by the access pattr generated circuit based on the comparator output.

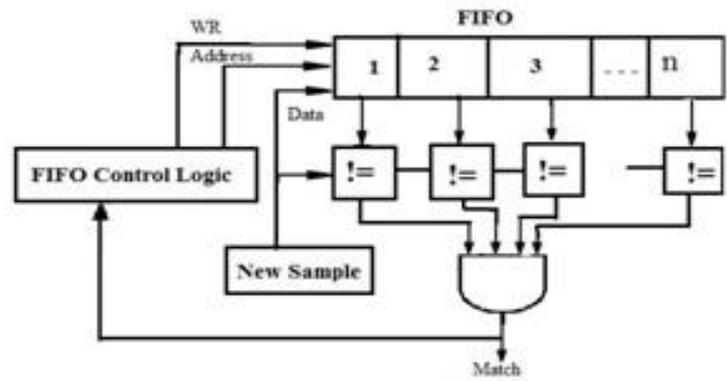


Figure2. Proposed design for bare histogram calculation

From the previous method we adopted the concept of the extracting the statistical values without effecting the operation of the histogram. In the statistical unit consists of two elements namely Multiplexer and priority encoder. Mux is used to determine present value of the concerned location. Priority encoder can be used for the calculation of the ratio of the samples occurred for the particular window size.

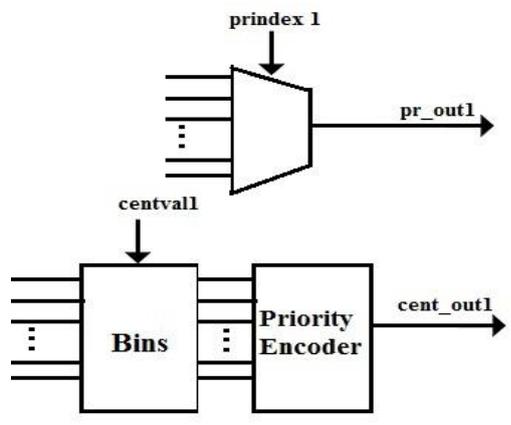


Figure3. Statistical unit

The operation of the priority encoder is, it provides the percentage of the sample occurrence. For example when A sample occurred 100 times then the output of the priority encoder will 10 centric. That means this will help the user to calculate the histogram and to perform the statistics very easily. By this without effecting the operation of the histogram calculating unit can extract the desired information at any time.

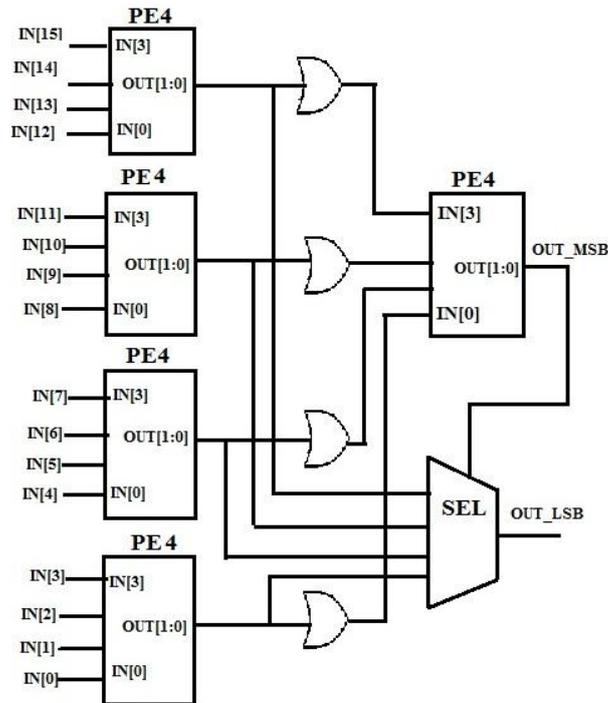


Figure4. Priority encoder

Priority encoder is designed by pipelining sub set of the 5- priority encoders and those will decide individual 4 combinations. When MSB is high then the most priority encoder can be deciding and that will generated output. Each will correspond to the upper priority encoder.

In our proposed parallel design of the histogram unit will gives the good result with concern to the area and the power also. But the important element only two clock cycles can be used for the production of the output.

#### 4. RESULTS AND DISCUSSION

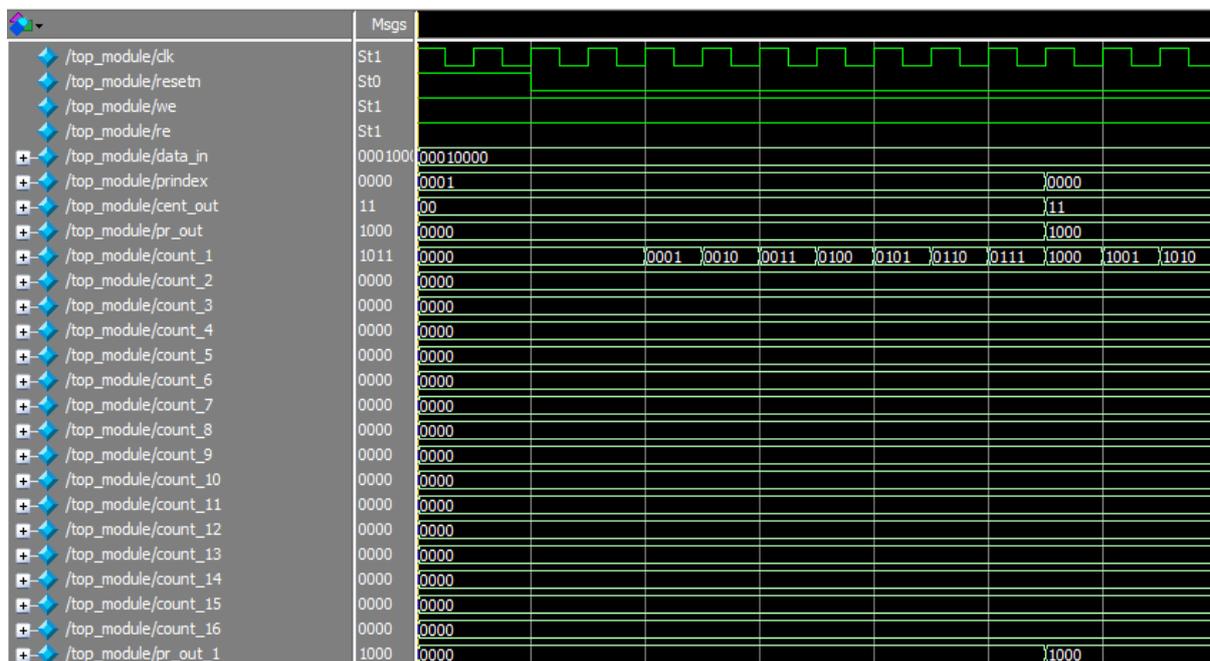


Figure5. proposed estimator output

The reset input reset n is applied '1' for initialize the all signals and memories and flip-flops data input we are not changed any input so the counter is incremented to 1 to 7 then we changed the prindex so it given the present count and centriel out as 1000(8), even though the data input were not changed so it being incrementing.

**Synthesis comparison of proposed and previous**

kernel Project Status (09/06/2015 - 16:35:25)			
Project File:	kernal.xise	Parser Errors:	No Errors
Module Name:	kernel	Implementation State:	Synthesized
Target Device:	xc3s500e-5fg320	• Errors:	No Errors
Product Version:	ISE 14.3	• Warnings:	<a href="#">1 Warning (1 new)</a>
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	<a href="#">Xilinx Default (unlocked)</a>	• Timing Constraints:	
Environment:	<a href="#">System Settings</a>	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	152	4656	3%
Number of Slice Flip Flops	148	9312	1%
Number of 4 input LUTs	199	9312	2%
Number of bonded IOBs	22	232	9%
Number of GCLKs	1	24	4%

**Figure6.** Previous Architecture Synthesis Report

top_module Project Status (09/06/2015 - 17:17:21)			
Project File:	histsynth.xise	Parser Errors:	No Errors
Module Name:	bare_his	Implementation State:	Synthesized
Target Device:	xc3s500e-5fg320	• Errors:	No Errors
Product Version:	ISE 14.3	• Warnings:	<a href="#">517 Warnings (32 new)</a>
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	<a href="#">Xilinx Default (unlocked)</a>	• Timing Constraints:	
Environment:	<a href="#">System Settings</a>	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	56	4656	1%
Number of Slice Flip Flops	57	9312	0%
Number of 4 input LUTs	70	9312	0%
Number of bonded IOBs	84	232	36%
Number of GCLKs	1	24	4%

**Figure7.** Proposed architecture synthesis report

The previous method consumed 3% utilization of the LUT's in the Spartan-3e architecture where as proposed method consumed less than 1% LUT's. From the above synthesis results we can declare that our proposed method utilizes less LUT's

Parameter	Previous	Present
No Of 4 input LUTS	199	70
Maximum output required time after clock	7.602ns	4.221ns
Minimum input arrival time before clock	7.292ns	6.014ns

**5. CONCLUSION**

We evidenced a new architecture for computing the PDF estimation for the real-time adoptive system with less latency methodology. Our proposed cumulative histogram with parallel operation can be increases the execution of statistical calculation. Even we adopted a method of extracting the data without effecting the operation of the mail unit. The added feature of our method the input bit length can be increases explicitly. With our architecture million samples can be considered for the calculation of the histogram per second more over we can increase the sample per second by increasing the clock frequency.

In future work, we explore the use of this architecture within adaptive systems, to understand the impact of design. We feel that this architecture can enable a range of new applications incorporating intelligent adaptation.

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