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Low Power and Area Efficient 128 Bit Carry Select Adder

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Abstract: *In most of the data processing processors to perform arithmetic functions Carry Select Adder (CSLA) is used as this is one of the fastest adders. In order to increase the overall efficiency of the processor we can reduce the area and power consumption of the CSLA of processors. Based on this we can modify the regular SQRT CSLA architecture as 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture. The proposed design has been reduced area and power as compared with the regular SQRT CSLA. This work evaluates the performance of the proposed designs in terms of delay, area, power. The results analysis shows that the proposed CSLA structure is efficient than the regular SQRT CSLA*

1. INTRODUCTION

Design of efficient high-speed data path logic systems are the most design areas of research in VLSI system design. In digital adders, the speed of addition is depends on the propagate a carry through the adder. The sum for each bit position in an adder is generates only after the last bit position has been sum and a carry propagates to the next bit.

The CSLA use more area because it uses two Ripple Carry Adders (RCA) to get sum and carry by taking carry input Cin = 0and Cin = 1, then the final sum and carry are select by the mux .In this work instead of RCA with Cin=1used Binary to Excess-1 Converter compare to regular CSLA to achieve low power consumption low area. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure

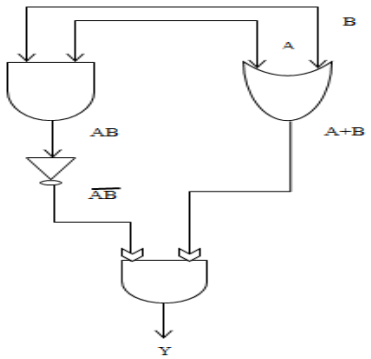


Figure: *Area evaluation of Exclusive OR gate*

2. CARRY SELECT ADDER

In the next modification of Regular CSLA, the RCA with Cin=1 & multiplexer, is replaced by combinational circuit, which consist of AND & XOR gate. Design of 16-bit modified CSLA without using mux is done [2]. It has five groups of different bit sizes. Initialy RCA structure calculates sum & carry for Cin=0, the output of full adder is given to the combinational circuit, one of the input of combinational circuit is previous stage carry. Then the final sum & carry is selected by combinational circuit to generate proper output [2]. But the disadvantage of this modified CSLA without using mux is that the delay is increased then Regular CSLA & modified CSLA using BEC [2]

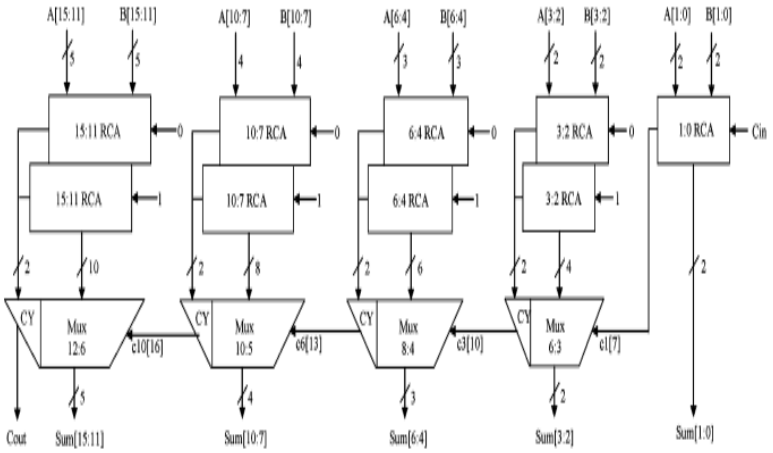


Fig.2. *Block Diagram of Regular 16bCarry Select Adder*

Carry lookahead adder (CLA) is also one of the fastest adder used in many data-processing processor. It takes lowest carry propogation delay, to generate final sum & carry output, but the disadvantage of CLA is this that it consumes larger area as compared to other adders

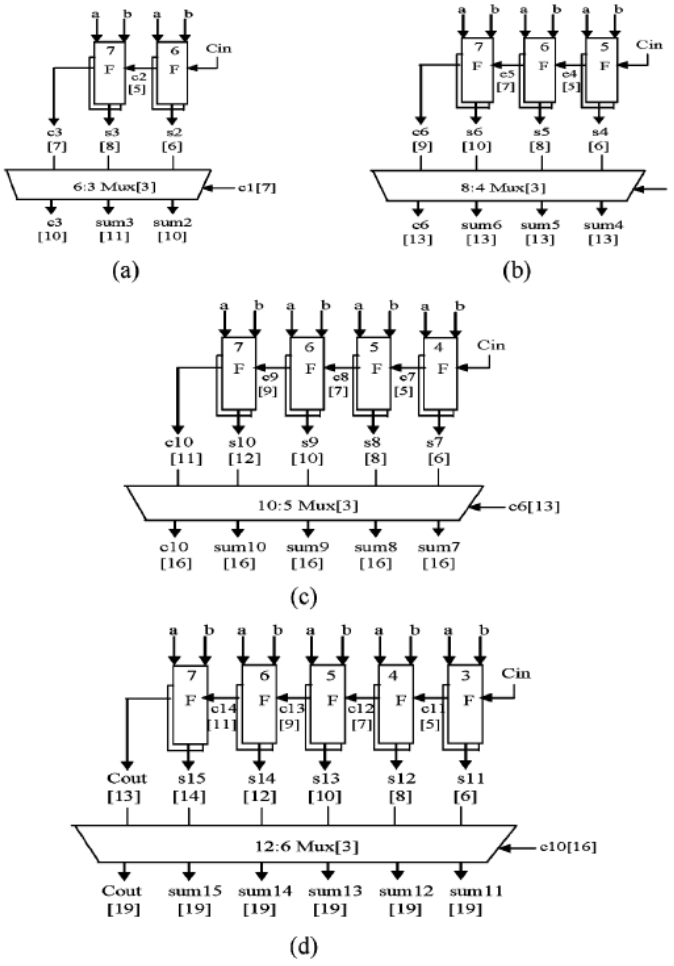


Figure 5. *Regular SQRT CSLA (a) group 2 (b) group 3 (c) group 4 and (d) group 5. F is full adder.*

3. EXCLUSIVE AREA EFFICIENT CSLA

The main idea of MA-CSLA is to use 4 gate XOR which reduces the total gate count. From the Figure 2 it is clear that there is the possibility of reduction of gates by using the XOR gates which has been proposed in our design. In the Modified CSLA the total number of XOR gates is 210.In Modified Area Efficient CSLA (MA-CSLA) the total number of XOR gates is 168.In the Modified Area

4. OPTIMIZED BEC

The XOR gate in BEC of Modified CSLA is replaced with the optimized XOR gate in AOI of Modified Area Efficient CSLA .With BEC there is reduction of gates by replacing n bit RCA with n+1 bit BEC[2].When the optimized XOR gate is used in Modified CSLA ,it is verified that there is large reduction in number of gates. The MUX is used to select either the BEC output or the inputs given directly to a BEC circuit[2].In this design, the major function of MUX is to derive the adder speed.

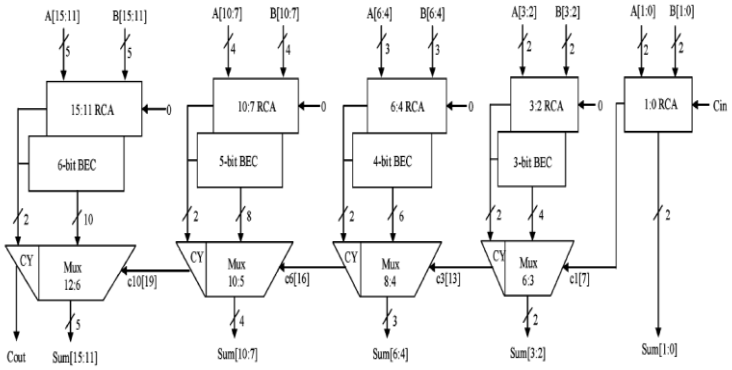


Figure 6. *Modified efficient carry select adder*

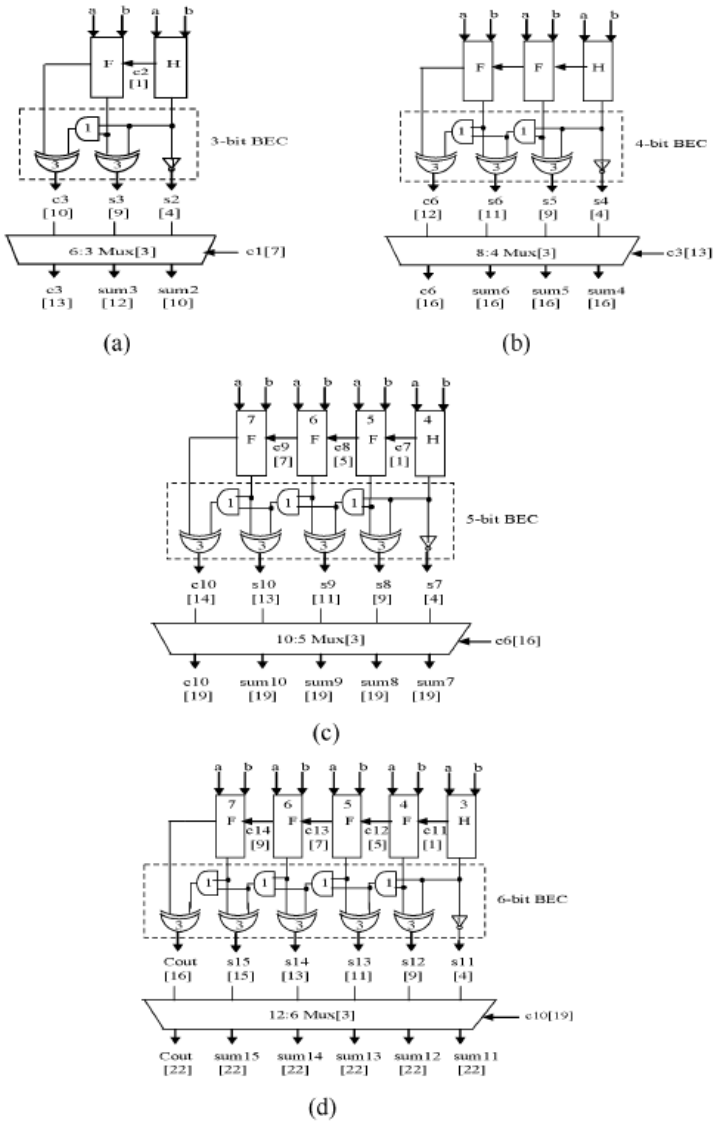
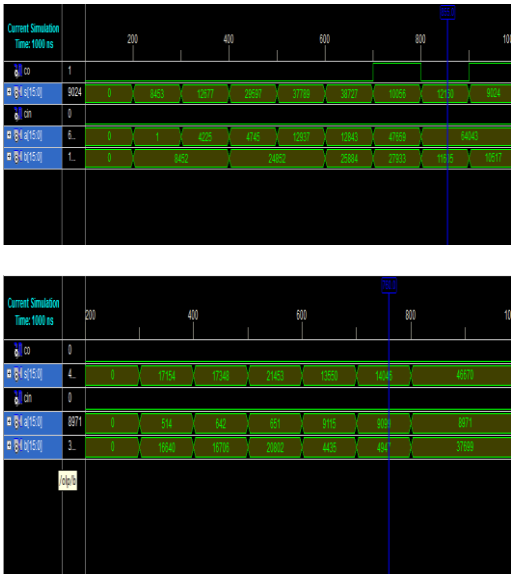


Figure 7. *Modified SQRT CSLA (a) group 2 (b) group 3 (c) group 4 and (d) group 5. F is full adder.*

5. FPGA IMPLEMENTATION RESULTS

The design proposed in MA-CSLA is successfully tested using (Xilinx) Spartan 3E series target and verilog HDL. The MA-CSLA architecture is simulated using isimulator. The result analysis of Modified CSLA (M-CSLA) and Modified Area efficient CSLA(MA-CSLA) is compared below



6. CONCLUSION

A proposed method in this paper reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work is advantage in the reduction of area and total power, compared results show that the modified SQRT CSLA has delay but the area and power of the 64-b SQRT CSLA are reduced by 15.4% and 11.4% respectively. The power-delay product and area-delay product of the proposed design indicates the success of the method and tradeoff of delay for power and area. The modified CSLA architecture is there-fore, low area, low power, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-b SQRT CSLA

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