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Clock Gating and Run Time Power Gating Integration by Using Dual Stacking Technique

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Abstract: *This Paper describes the facility Gating duration system that contains of temporal arrangement components like flip flops, latches and clock distribution network. This paper enumerates power economical style of shift registers victimization D flip flops alongside Clock and Power gating integration. Clock gating and power gating proves to be terribly effective solutions for reducing dynamic and active leak power severally. The 2 techniques area unit coupled in such the simplest way that the clock gating data is employed to drive the management signal of power-gating electronic equipment. During this paper, associate degree activity driven fine-grained clock and power gating is projected. First, a method named Optimized Bus-Specific-Clock-Gating (OBSC) is introduced that reduces the matter of gated flip-flop choice by applicable choice of set of flip flops. Then another technique named Run Time Power Gating (RTPG) is projected for power gating the combinable logics playing redundant operations. The projected Integration of Clock gating and Run Time Power gating with Stacking Technique T-Spice simulations for totally different clock frequencies and also the performance of the shift registers area unit evaluated by perceptive the typical power consumption.*

Keywords: *Optimized Bus-Specific-Clock-Gating (OBSC), Run Time Power Gating (RTPG), Stacking method.*

1. INTRODUCTION

Today's consumer demands more functionality, energy efficient device and optimized power devices as time goes, so in order to optimize power of a device the simplest control technique is to shut off the clock of the sequential block of the device when there is no function required from that section for some duration With the smaller geometries in Deep Sub-Micron (DSM) technology, the number of gates that need to be integrated on a single chip, power density, and total power are increasing rapidly. The scaling of process technologies to nanometer regime has resulted in a rapid increase in leakage power dissipation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground) . This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance .Power gating results in a reduction in leakage because when the sleep transistor is off, the virtual ground rail charges up to a steady state value close to VDD. However, it also has a drawback that while switching back to the active mode from the sleep mode, the virtual ground rail takes a long time to discharge through the sleep transistor. This results in a significant wake-up latency and wake-up power penalty and limits overall leakage savings by limiting how often a logic block can go in and out of the sleep mode. Clock Gating is a technique that can be used to control power dissipated by Clock net. In synchronous digital circuits the clock net is responsible for significant part of power dissipation (up to 40%) [2]. Clock gating reduces the unwanted switching on the parts of clock net by disabling the clock. Thus, it seems prudent to have multiple sleep modes that trade-off wake up penalty for leakage savings. During a stretch of inactivity, the processor can go into one of the intermediate sleep modes as determined by the wake-up overhead and save power without degrading performance. Unlike conventional power gating, the multiple sleep mode capability also provides an option of state-retentive mode to enable power savings during inactive periods while preserving the state of the circuit CMOS digital circuits occurs in two forms: dynamic and static. Dynamic power dissipation occurs in the l ogic gates that are in the process of switching from one state to another. During this process, any internal and external

capacitance associated with the gate's transistors has to be charged, thereby consuming power. Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another). Dynamic power is important during normal operation, especially at high operating frequencies, whereas static power is more important during standby, especially for battery-powered devices for dynamic loss reduction we are using Clock Gating technique and for static loss reduction we are suing RTPG technique explained below.

2. CLOCK GATING AND POWER GATING

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of muxes and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree.

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

3. INTEGRATED CLOCK AND POWER GATING

Clock Gating and Power Gating are two most commonly used design methods to save dynamic and leakage power respectively. How about integrating the two solutions such that they complement each other? In this post, I will talk about a simple way to do so.

Clock Gating is accomplished by using Clock Gating Integrated Cell *(CGIC)* which gates the clock to the sequential elements present in its fan-out when the enable signal is logic 0. Power gating structures may be of two types: Simple Power Gating and State Retention Power Gating. Using the former technique, the output of the logic gates slowly leaks the charge at the output and thereby when the *SLEEP* signal is de-asserted, one cannot predict the logic value at the output. The latter technique is able to retain the state at the output which was last present before asserting the *SLEEP* signal.

Let's take up a few plausible scenarios:

- Case I - Normal Case: This employs only conventional clock gating. It is depicted in the figure.

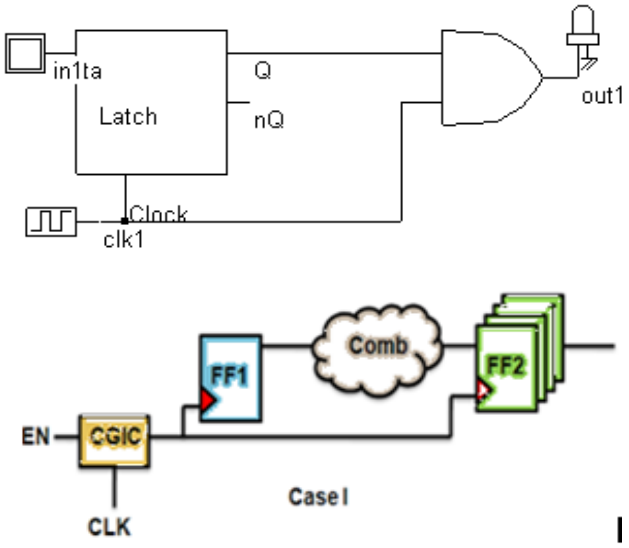


Fig 3.1. *Clock Gating Integrated Cell*

- Case II - When one does not need to retain the states of the combinatorial cells or the sequential elements. One possible scenario could be in the case of a standalone IP, which is not communicating with any other IP on the SoC. Here one can use the simple power gating where the SLEEP signal is derived from the CGIC itself using a latch, as depicted in the figure below. Doing so, we would save both dynamic and leakage powers.

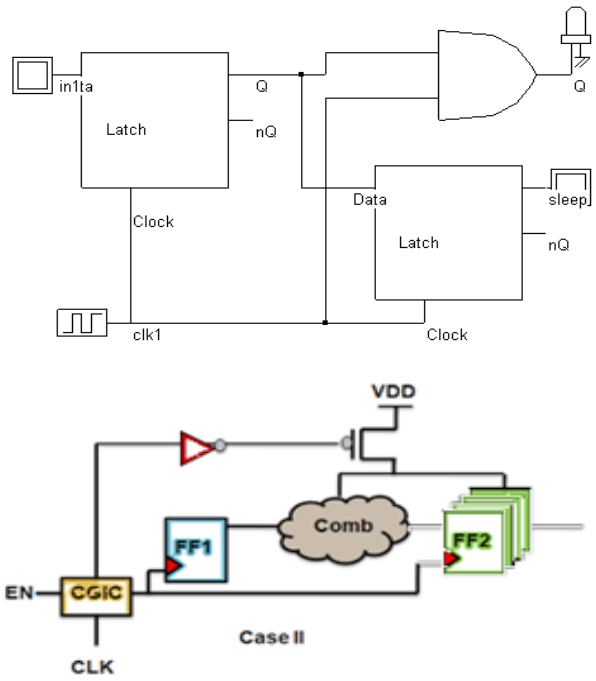
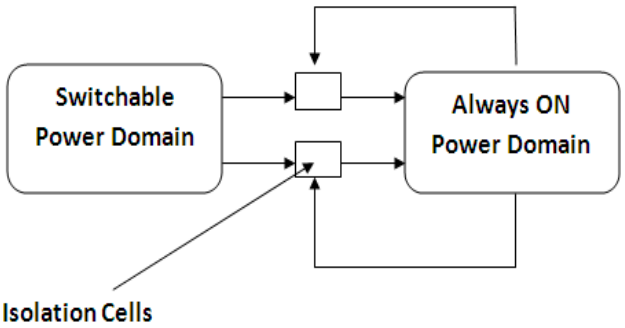


Fig 3.2. *Modified clock Gating Integrated Cell*

- Case IIII - When one does not need to retain the states of the combinatorial cells, but the sequential outputs need to be safe-stated. Possible use-case could be where only the sequential outputs communicate with other IPs on the SoC. This can be accomplished by using State Retention Flip Flops instead of the conventional flip-flops.
- Case IV - When both the combinatorial cells and the sequential cells interact with other IPs. But the previous value need not be required. Since it is a classic case of interaction between "switchable power domain" with" always ON", it entails the use of isolation cells between such power domain crossings. It must be noted that in such a case, isolation cell would always be present in the always ON power domain, i.e., it would receive its VDD supply from the always ON power domain supply. This is because, when the switchable power domain in OFF, the isolation cell can function only if receives the power supply!



Isolation Cells can be simple cells like AND or an OR gate, which receive one input in a way that, irrespective of the second input coming from the switchable power domain, the value would be controllable. For example, logic 0 for AND gate and logic 1 for an OR gate. I will try to take this up in a separate post.

Here we classified the shift register to three places

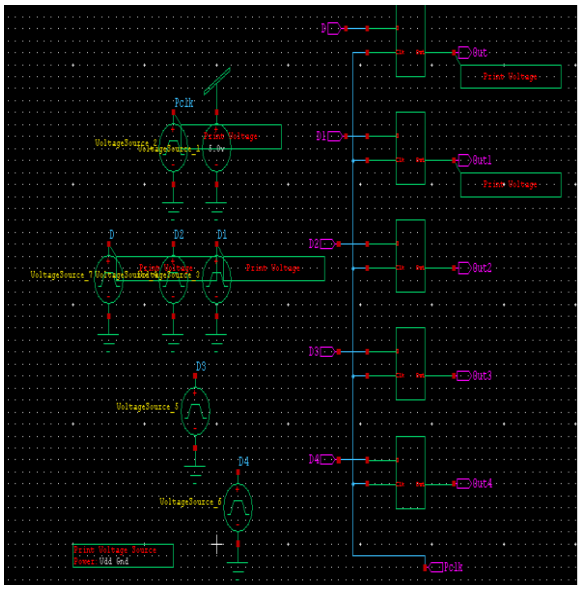


Fig3.3. *Non Clock Gating Circuit.*

4. OBSC TECHNIQUE

Optimized Bus Specific Clock Gating is very effective technique to maximize dynamic power reduction as shown in fig.3. It chooses only a subset of flip-flops (FF) to be gated selectively, and the problem of gated FF selection is reduced from exponential complexity into linear. It works by comparing the inputs and outputs and gates the clock when they are equal. Considering N FFs in the non-CG circuit, each FF can be chosen as gated or non gated. Hence, 2N CG solutions are possible and the exponential complexity problem is reduced into linear. Assume that all the FFs are chosen to be gated initially, and then the problem is in determining which FFs should be excluded from gating. Heuristically, the FF with the maximum output data toggle rate should be excluded from gating first. This is because that maximum output data toggle rate indicates that minimum clock toggles will be gated, thus power will reduce least or even increase if the FF is gated. More formally, the FF with the maximum output toggle rate is excluded from gating first, then the FF with the second largest output toggle rate is excluded and so on until all the FFs are excluded (i.e., the original non CG circuit). Apparently, during the process of exclusion, there will be N+1 possible CG solutions which is linear complexity.

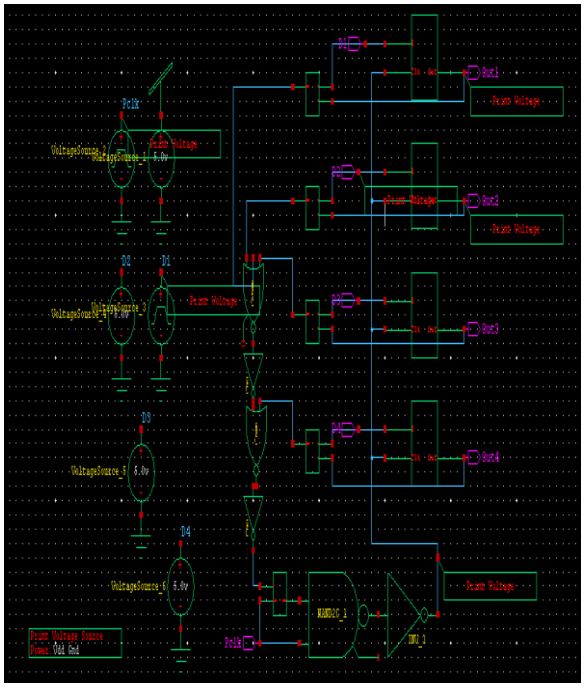


Fig4.1. *PBSC circuit*

In order to achieve integration of CG and RTPG, apply OBSC technique to the design, then a subset of FFs is clock gated. During the clock gated period, the outputs of the gated FFs are stable. Consequently, those combinational logics whose inputs only depend on gated FF outputs will be inactive and can be power gated as shown in Fig 6.(a). For each output of the power gated cell, whether a connection to primary output presence has to be checked. A holder logic should be added in order to avoid signal floating. Suppose that four out of five FFs are clock gated. The circled cells are completely dependent on the stable gated FF outputs, so they are not active and can be power gated into sleep [1]. However, one input of the XOR gate i is the output of ungated FF A, and one input of the AND gate h is the primary input. Since both the ungated FF output and PI may not be stable during the clock gated period, the XOR gate i and the AND h may be active. So they should not be power gated. In order to avoid floating signal, a holder should be placed at the output of each power gated cell if that output connects to non power gated cells or primary outputs (Pos)

If RTPG has to be applied, a footer (high-Vth CMOS transistor) between the actual ground and virtual ground of the power gated cells should be added. After the integration of CG and RTPG, the low power design should look like Fig.6 (b).The enable signal generated from OBSC is used as the sleep signal for the PG. The cells that are totally dependent on gated FF outputs are power gated. Holders are placed between the power gated cells and the non power gated cells so that the non power gated cells can function properly

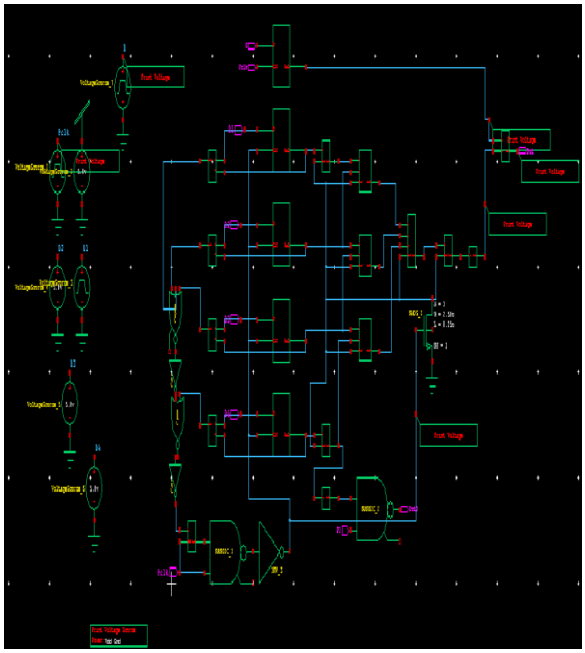


Fig4.2. *Integration of OBSC and RTPG*

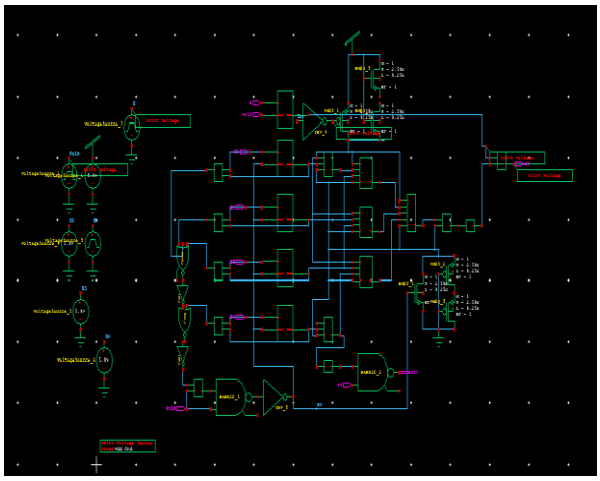
If RTPG has to be applied, a footer (high-Vth CMOS transistor) between the actual ground and virtual ground of the power gated cells should be added. After the integration of CG and RTPG, the low power design should look like Fig.6 (b).The enable signal generated from OBSC is used as the sleep signal for the PG. The cells that are totally dependent on gated FF outputs are power gated. Holders are placed between the power gated cells and the non power gated cells so that the non power gated cells can function properly.

5. PROPOSED TECHNIQUE

The stack approach combines the sleep and stack approaches the sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Area penalty is a significant matter for this approach since every transistor is replaced by three transistors. Here sleep transistors M 1 and M2 are stacked.

When in standby mode i. e. When MI and M2 both are off. In this structure firstly, the leakage current is reduced by stacking effect, turning both M 1 and M2 sleep transistors OFF. This raises the intermediate node voltage VGN to positive values to small drain current. In the analyzed scheme, the leakage current is reduced by the stacking effect, turning both Ml and M2 sleep transistors OFF. This raises the intermediate node voltage VGND2 to positive values due to small drain current.

During sleep to active mode transition, transistor M I is turned ON and transistor M2 turned ON after a small duration of time (IH). The logic circuit is isolated from the ground for a short duration as the transistor M2 is turned OFF. During this duration, the GBN can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor M2 in triode region.



Integration of OBSC and RTPG withDual stack Technique

Tabulation:

Circuit	Power Dissipaion
Integration of OBSC and RTPG with sleep	4.113243e-002 watts
Integration of OBSC and RTPG with Dual Stack Technique	4.400130e-003 watts

6. CONCLUSION

In this Paper, a fine-grained CG and RTPG integration is achieved in sequential circuits. First, an activity driven fine-grained OBSC technique is evaluated that selects only a subset of FFs to gate. Moreover, the clock enable signal generated in the OBSC circuit can be used as the sleep signal in RTPG. Following this, Sequential circuits that implements both OBSC and RTPG is considered and their performances are evaluated with sleep and stack ing technique.

REFERENCES

[1] Li Li, Ken Choi, and Haiqing Nan , “Activity-Driven Fine-grained Clock Gating and Run Time Power Gating Integration”, IEEE transactions on very large scale integration (VLSI) systems, vol. 21, no. 8, August 2013.

[2] S.M.Kang,Y.Leblebici, Ed. , “CMOS Digital Integrated Circuits analysis and design”. Third Edition, TMH, 2003

[3] M.Morris Mano,Michael D.Ciletti, , “ Digital Design”, Fourth Edition, Pearson Education Inc

[4] Christian Piguet , “Low power CMOS Circuits”, Technology, Logic Design and CAD tools,Taylor and Francis Group 2006”

[5] J.S.Wang.P.H.Yang, “A Pulse Triggered TSPC FF for High speed, Low power VLSI design Applications” IEEE, 1998

[6] Neil H.E Weste,Kamran Eshraghian, “Principles of CMOS VLSI Design,” A Systems Perspective,Second Edition,Pearson Education Inc ,2002

[7] K. Usami and N. Ohkubo, “A design approach for fine-grained run-time power gating using locally extracted sleep signals,” in Proc. Int. Conf.Comput. Design, 2006, pp. 151–161

[8] L. Bolzani, A. Calimera, A. Macii, E. Macii, and M. Poncino, "Enabling concurrent clock and power gating in an industrial design flow," in Proc.Des. Autom. Test Eur. Conf., 2009, pp. 334–339

[9] K. Roy, S. Mukhopadkyay, and H. Mahmoodi-meimand, "Leakage current mechanisms and leakage reduction techniques in dee psubmicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327,Feb. 2003.

[10] Y. Tsai, D. Duarte, N. Vijaykrishnan, and M. Irwin, "Characterization and modeling of run-time techniques for leakage power reduction," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 11, pp. 1221– 1233, Nov. 2004.

[11] P. Babighian, L. Benini, and E. Macii, "A scalable algorithm for RTL insertion of gated clocks based on ODCs computation," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 24, no. 1, pp. 29–42, Jan. 2005.

[12] Andrew B.Kahng,Seokhyeong Kang,Bongil Park,"Active-Mode Leakage Reduction with Data-Retained Power Gating"Proc EDAA,2013